



## A RELATIONSHIP BETWEEN INTERFACE TRAP DENSITY AND TRANSCONDUCTANCE IN 6H-SiC ENHANCEMENT MODE FIELD-EFFECT TRANSISTORS

M. W. DRYFUSE and M. TABIB-AZAR

Electrical Engineering and Applied Physics Department, Case Western Reserve University, Cleveland, OH 44106, U.S.A.

(Received 17 November 1995; in revised form 11 January 1996)

**Abstract**—An explicit analytical expression relating the interface trap densities and transconductance is derived for enhancement mode field effect transistors without any simplifying assumptions regarding the energy distribution of traps. Using this relationship, the interface trap densities were calculated from the experimental transconductance data and compared with experimental data and that provided in the current literature. Interface states are important material surface characteristics that may significantly affect the device behavior. Our expression provides a simple and convenient method to reliably estimate interface trap densities from the readily available transconductance data provided in the pertinent literature. Copyright © 1996 Elsevier Science Ltd

### 1. INTRODUCTION

Except in silicon, where interface trap densities of SiO<sub>2</sub>/Si system are reduced below 10<sup>10</sup> eV<sup>-1</sup> cm<sup>-2</sup>[1], field-effect transistors of other semiconductors like GaAs and *p*-type 6H-SiC are plagued by large densities of interface traps, in excess of 10<sup>11</sup> eV<sup>-1</sup> cm<sup>-2</sup>[2]. Owing to its high breakdown field strength (~3 × 10<sup>6</sup> V · cm<sup>-1</sup>), radiation hardness, and large energy band gap (3.0 eV), that makes it a desirable material for high temperature and power device applications, SiC has received considerable attention in recent years[3]. The native oxide of the SiC is in the form of SiO<sub>2</sub> and produces acceptable interface trap densities in *n*-type nitrogen doped 6H-SiC (<10<sup>11</sup> eV<sup>-1</sup> cm<sup>-2</sup>)[4]. However, in *p*-type samples, both aluminum and boron doped, the interface trap densities are quite large and need further studies and research to be improved.

Interface states came to the attention of early investigators such as Shockley, Tamm and others who were trying to design field effect transistors on Ge and Si[5–7]. In the course of their studies it became apparent that large densities of surface states in these materials shield the externally applied electric field from modulating of the channel conductance in FETs. Moreover, it was also discovered that these states change their charge content as a function of the ambient gases causing instabilities in the device behavior. Because of these problems, surface based devices such as FETs and planar technologies had to wait for successful passivation of the silicon devices. Simply put, these states can be viewed as electronic states generated by unsaturated dangling bonds of the surface atoms[6]. In the laboratory environment,

crystal surfaces are usually covered with layers of native oxides and organic contaminants, and surface states in the presence of these layers are modified and referred to as “interface states”.

While interface traps are undesirable both in minority and majority carrier devices, they can be fatal in some majority carrier devices by pinning the Fermi-level and disabling the field effect. Even when the interface trap densities are not large enough to pin the Fermi-level, they can deteriorate the ability of an external electric field to modulate the channel conductance in FETs. The deterioration of the field effect is directly reflected in the transistor's transconductance which is a measure of the strength of the field effect. Many SiC FETs have been reported in the literature, but problems still persist in producing a device with large transconductances. Low transconductances in these devices may be due to a combination of factors such as large contact resistances, micropores[8], and interface traps to name a few. Therefore, the relationship derived can provide insight into the interface state traps impact on the experimental transconductance as it relates to SiC enhancement mode MOSFETs.

A relationship between the interface trap densities and transconductance for depletion mode field-effect transistors was derived and tested before[9]. Here we extend this analysis and solve for a similar relationship in enhancement mode field-effect transistors. In an attempt to compare results with the ones reported in the literature, we have discovered that most researchers report either  $g_{m,s}$  or  $D_{it,s}$ , and these are rarely reported simultaneously. There is also a question regarding what levels of  $D_{it,s}$  are

acceptable from a device operation point of view. Finally, we wanted to know how the combination of insulator capacitance, and channel doping level can be altered to offset the effect of the interface traps on  $g_m$ , and to obtain a simple design rule regarding these parameters. Our motivations in the present study, therefore, are: (i) estimate  $D_{it}$  given  $g_m$  and *vice versa*, (ii) determine the importance of the interface traps in reducing  $g_m$  and (iii) develop simple rules in designing SiC enhancement mode FETs.

Furthermore, one of the interesting and important questions in device modeling, in general, is how device parameters are affected by that of the materials? Using numerical methods it is not very difficult to incorporate material parameters in the equations governing the device behavior and numerical methods are routinely used by most researchers in the field. However, it is almost universally accepted that numerical methods are not effective tools in developing an overall picture and intuition regarding the device behavior. On the other hand, closed form relationships are usually derived using many simplifications that, in some cases, render them ineffective in explaining the device behavior. More often, however, simple closed form analytical relationships help us to develop a mental picture of the underlying processes. Transconductance and interface trap densities are commonly measured to characterize devices, and are widely reported in the literature. The relationship that is derived in the present work enabled us to make direct comparison between the ideal transconductance and its experimental value taking into account trap densities.

## 2. THEORETICAL CONSIDERATIONS

Interface states are fast or slow, denoted by  $D_{itf}$  and  $D_{its}$ , respectively, depending on their ability to follow fast or slow signals. Here we shall investigate the behavior of the MOSFET transconductance in the presence of fast and slow traps under d.c. conditions.

### Direct current relationship

We consider an  $n$ -channel enhancement mode device, but the derivation here can easily be adapted for a  $p$ -channel device. The gate voltage is the sum of the insulator voltage ( $V_i$ ) and the semiconductor surface potential ( $\Psi_s$ ) in a metal oxide semiconductor device. The insulator voltage is given by:

$$V_i = \frac{Q_{sc}}{C_i}$$

where  $C_i$  is the insulator capacitance and  $Q_{sc}$  is the semiconductor charge. From Poisson's equation the semiconductor charge is related to the semiconductor potential by [10]

$$Q_{sc} = \frac{\sqrt{2\epsilon_s kT}}{C_i q L_D} F\left(\beta\Psi_s, V, \frac{n_{po}}{p_{po}}\right), \quad (1)$$

where

$$F\left(\beta\Psi_s, V, \frac{n_{po}}{p_{po}}\right) = \left[ e^{-\beta\Psi_s} + \beta\Psi_s - 1 + \frac{n_{po}}{p_{po}} e^{-\beta V} (e^{\beta\Psi_s} - \beta\Psi_s e^{\beta V} - 1) \right]^{1/2}$$

and  $\beta = \frac{q}{kT}$

$V$  is related to the drain voltage. Also  $L_D$  is defined as the extrinsic Debye length for holes and is given by:

$$L_D = \sqrt{\frac{\epsilon_s}{qp_{po}\beta}}$$

Also,  $n_{po}$  and  $p_{po}$  are given by

$$n_{po}p_{po} = n_i^2, \quad p_{po} \cong N_A.$$

(Actually this last relationship that assumes all of the dopants are ionized, is a poor assumption for deep acceptors such as boron and aluminum in 6H-SiC at room temperature.) The charges in the interface traps result in an additional voltage drop across the insulator. Denoting this interface trap voltage by  $V_{it}$  we can write:

$$V'_g = V_g + V_{it} + R_{SG}I_{DS} \quad (2)$$

$V_{it}$  is furthermore related to the interface-states trap charges ( $Q_{it}$ ) by

$$V_{it} = \frac{Q_{it}}{C_i}, \quad (3)$$

where  $Q_{it}$  is determined by the integral of the interface-state trap density ( $D_{it}$ ):

$$Q_{it}(\Psi_s) = q \int_{E_s}^{E_f + \Psi_s} D_{it}(E) dE, \quad (4)$$

where  $D_{it} = D_{its} + D_{itf}$ , and the slow traps are assumed to have reached equilibrium.

Transconductance is determined by changing the gate voltage and measuring the drain current at a fixed drain voltage

$$g'_m = \left. \frac{\partial I_{DS}}{\partial V'_g} \right|_{V'_{DS} = \text{const}}, \quad (5)$$

where  $V'_g$  is the bias between the gate and the channel. Differentiating eqn (2) with respect to  $I_{DS}$  and remembering  $V_{it}$  is a function of  $\Psi_s$ , yields:

$$\frac{\partial V'_g}{\partial I_{DS}} = \frac{\partial V_g}{\partial I_{DS}} + \frac{\partial V_{it}}{\partial \Psi_s} \frac{\partial \Psi_s}{\partial I_{DS}} \frac{\partial V_g}{\partial I_{DS}} + R_{SG}. \quad (6)$$

Furthermore, we have:

$$\frac{\partial \Psi_s}{\partial V'_g} = \left( -\frac{\partial Q_{sc}}{\partial \Psi_s} + \frac{\partial \Psi_s}{\partial \Psi_s} \right)^{-1}.$$

Table 1. Calculated ideality factor for SiC FETs with different channel doping and interface trap densities at different surface potentials using eqn (9) ( $C_{ox} = 8.3 \times 10^{-8} \text{ F cm}^{-2}$ )

$N_A \text{ (cm}^{-3}\text{)}$	$D_{it} \text{ (eV}^{-1} \text{ cm}^{-2}\text{)}$	$1 \times 10^9$	$1 \times 10^{10}$	$1 \times 10^{11}$	$1 \times 10^{12}$	$1 \times 10^{13}$
		$\eta$	$\eta$	$\eta$	$\eta$	$\eta$
(at 300 K)	$\Psi_s \text{ (V)}$					
$1 \times 10^{-14}$	1.18	0.998	0.982	0.843	0.349	0.051
$1 \times 10^{-16}$	1.33	0.999	0.987	0.885	0.435	0.071
$1 \times 10^{-18}$	1.42	1.000	0.955	0.906	0.656	0.160
(at 900 K)						
$1 \times 10^{-14}$	1.08	0.998	0.982	0.847	0.356	0.052
$1 \times 10^{-16}$	1.97	0.999	0.990	0.902	0.480	0.084
$1 \times 10^{-18}$	2.52	1.000	0.996	0.963	0.721	0.205

By using the definitions of  $g_m$  and  $g'_m$  we have:

$$g'_m{}^{-1} = g_m^{-1} + \frac{\partial V_{it}}{\partial \Psi_s} \frac{\partial \Psi_s}{\partial V_g} g_m^{-1} + R_{SG}. \quad (7)$$

Evaluating this expression with eqns (1), (2) and (4) gives:

$$g'_m{}^{-1} = g_m^{-1} + \frac{q^2 D_{it}}{C_i} \times \left\{ K \frac{\left[ 1 - e^{-\beta \Psi_s} + \frac{n_{po}}{p_{po}} e^{\beta V} (e^{\beta \Psi_s} - e^{\beta V}) \right]}{F\left(\partial \Psi_s, V, \frac{n_{po}}{p_{po}}\right)} + 1 \right\}^{-1} g_m^{-1} + R_{SG}, \quad (8)$$

where

$$K = \frac{\epsilon_c}{\sqrt{2} C_i L_D}$$

An ideality factor ( $\eta$ ) can be defined by setting  $R_{SG}$  equal to zero and is given by:

$$\eta = \frac{g'_m}{g_m} = \left\{ 1 + \frac{q^2 D_{it}}{C_i} \times \left\{ K \frac{\left[ 1 - e^{-\beta \Psi_s} + \frac{n_{po}}{p_{po}} e^{-\beta V} (e^{\beta \Psi_s} - e^{\beta V}) \right]}{F\left(\beta \Psi_s, V, \frac{n_{po}}{p_{po}}\right)} + 1 \right\}^{-1} \right\}^{-1}$$

for  $(\Psi_s > 0)$ . (9)

This relationship applies to cases where the drain voltage is nonzero. From this general equation, we can identify some device parameters relating to transconductance. We directly see that as the interface state density is increased,  $\eta$  decreases. By reducing the oxide layer thickness, we can increase the oxide capacitance, which in turn limits the interface state effect. Also,  $\beta$  clearly shows the temperature dependence.

Now before we turn to the experimental data, we plug in some known material values for SiC into our general (without correcting for  $R_{SG}$ ) expression to get a feel for how it will behave. We do this for SiC at temperatures of 300 and 900 K at various doping levels which are listed in Table 1, where values for  $\eta$  as a function of the interface states are shown. From the listing in Table 1 we deduce some preliminary characteristics. The most important characteristic to note is how rapidly  $\eta$  changes over the range of interface states from approximately  $1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  to  $1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$  for dopings between  $10^{16}$  and  $10^{18} \text{ cm}^{-3}$ .

The expression suggests that if we increase the carrier concentration to relatively large values, we should be able to reduce the effect of interface states on the transconductance. This will happen only if the doping itself does not contribute to the interface state densities.

In the case of relatively deep dopants, such as aluminum and boron in SiC, this may not be correct and it has been demonstrated that indeed increasing the  $p$ -type doping level in 6H-SiC, increases its interface trap densities[4].

### 3. EXPERIMENTAL DATA

We have currently applied this relationship to 6H-SiC enhancement mode MOSFETs provided by

 Table 2. SiC devices parameters used in the present work (in 6H-SiC:  $n_i = 1.6 \times 10^{-6} \text{ cm}^{-3}$ ,  $\epsilon_s = 8.55 \times 10^{-13} \text{ F cm}^{-2}$  and  $E_g = 3.0 \text{ eV}$ )

Parameters	Device 1	Device 2	Device 3
$C_i \text{ (F cm}^{-2}\text{)}$	$7.8 \times 10^{-8}$	$8.3 \times 10^{-8}$	$8.3 \times 10^{-8}$
$N_A \text{ (cm}^{-3}\text{)}$	$3 \times 10^{-16}$	$3 \times 10^{-16}$	$3 \times 10^{-16}$
$L \text{ (}\mu\text{m)}$	8	4	8
$Z \text{ (}\mu\text{m)}$	100	100	12
$V_{FB} \text{ (V)}$	2.0	2.1	2.0
$V_T \text{ (V)}$	2.5	2.3	2.5
$\mu_{eff} \text{ (cm}^{-2} \text{ V}^{-1} \text{ s}^{-1}\text{)}$	20	22	20
$d \text{ (}\text{\AA}\text{)}$	443	416	443

## Interface Trap Density vs Surface Potential

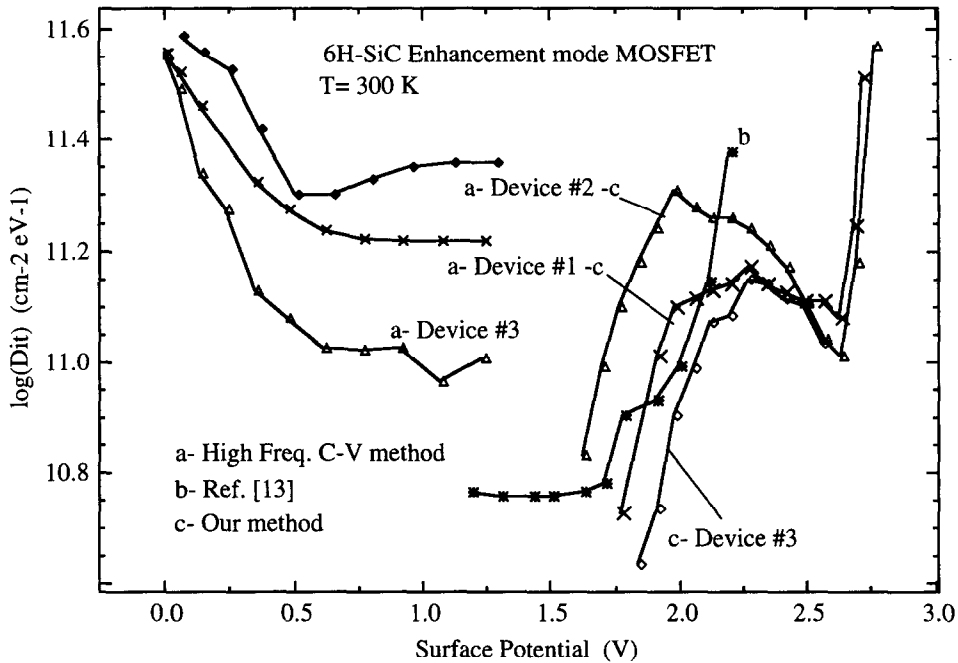


Fig. 1.  $D_{it}$  vs surface potential for 6H-SiC  $n$ -channel enhancement mode MOSFET numbers 1, 2 and 3.

CREE Research Inc.[11]. The device parameters we used in our calculation were based on  $C-V$  and  $I-V$  measurements and material values that are summarized in Table 2. We obtained our own data based on the simple approximation using high frequency  $C-V$  measurements[1] using a Keithley 590  $C-V$  Analyzer. Whenever needed (namely, over the region where the high frequency method failed to give interface states), we used the data reported in Ref. [12] to compare with our transconductance results.

The transconductance data was determined from  $I-V$  measurements performed using a Hewlett Packard 4541B Semiconductor Parameter Analyzer. From the  $I-V$  measurements, we were able to extract the experimental transconductance and obtain values for the effective carrier mobility. It is also important to note that we converted from gate voltage to surface potential via:

$$V_g = \frac{\sqrt{2}\epsilon_s}{C_i L_d \beta} F\left(\Psi_s, V, \frac{n_{po}}{p_{po}}\right) + \Psi_s, \quad (10)$$

The theoretical transconductance is calculated based on the following simple relation for the saturation region:

$$g_m = \frac{Z}{L} \mu_{eff} C_i (V_g - V_T), \quad (11)$$

where  $Z$  and  $L$  are the device width and channel length, respectively.  $V_T$  is the threshold voltage and  $\mu_{eff}$  is the effective channel mobility. The effective channel mobility remains one of those quite difficult

values to determine. This is because the three different parameters of  $D_{it}$ ,  $R_{sg}$  and  $\mu_{eff}$  all have the same types of contribution to  $g_m$  at low frequencies. Here we will use:

$$\mu_{eff} \approx \frac{Lg_d}{ZC_i(V_g - V_T)}, \quad (12)$$

where  $g_d$  is the drain transconductance measured at 50 mV[18]. We propose that one calculates  $\mu_{eff}$  from  $V_T$  to strong inversion and take the average of these values. This will undoubtedly introduce some errors, but will provide an adequate value to estimate the interface trap density. The effective mobility values are listed in Table 2.

Using the above method to determine mobility, one can proceed to back-calculate the theoretical transconductances at a given surface potential (gate voltages). One can then compute each  $\eta$  by dividing the experimental transconductance by the theoretically obtained results. With  $\eta$  known, one can easily solve our expression for the interface trap density. If desired, eqn (9) can be modified to incorporate the effect of nonzero  $R_{sg}$ .

We can compare our calculations of the interface trap densities to representative values reported by Ref. [13] and for device 1 shown in Fig. 1. The interface trap density calculated from the transconductance data shows the ability to extend interface trap density values closer to the conduction edge on the bandgap where  $C-V$  and quasi-static methods breaks down. Based on our data we calculated an average  $D_{it}$  of  $1.2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ .

Figure 1 also displays the data for devices 2 and 3. Based on the above method, we were able to obtain interface trap densities of  $1.4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  for device 2 and  $9.9 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  for device 3.

The current literature provides a growing picture as to the nature of interface traps in SiC. Some reports have shown that  $D_{it}$ s are on the order of  $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  [4,13], which is unacceptable for good device performance. Our values seem to compare well to those reported by groups who place  $D_{it}$ s around a more acceptable range in the low  $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  [12,14–16]. This is primarily due to improved device fabrication techniques. It has also been shown that there still remain other problems, such as surface potential fluctuations, that may lead to discrepancies in determining accurate values for interface state densities based on conductance and capacitance techniques [17]. Therefore, our method gives one more measure of interface state density based on more easily obtainable transconductance data.

The three devices examined here allow for some general comments on our method's ability to estimate interface traps. After strong inversion, the interface density influence becomes negligible due to the exponential nature of the inversion charge. One should find that the expression breaks down near threshold, which is primarily due to eqn (10) becoming more inaccurate.

A drawback of our method is that one must accurately determine three key device parameters which are  $C_i$ ,  $V_T$ , and  $\mu_{\text{eff}}$ . This brings up the point that care must be taken to accurately calculate the theoretical transconductance based on reliable device parameters. For example,  $C_i$  may not be readily available, and it should be obtained from additional  $C-V$  measurements or device geometry. Also the pertinent literature should provide  $C_i$  or the geometry directly.  $C_i$  is a critical parameter in relating gate voltage to surface potential, and  $V_T$  dominates the determination of the theoretical transconductance and mobility calculations, but a number of accurate methods to determine  $V_T$  are described in Ref. [18].

Finally the most difficult task is determining  $\mu_{\text{eff}}$ . Many report  $\mu_{\text{eff}}$  based on taking the slope of the drain current vs gate voltage which can result in an effective carrier mobility. The problem we see in the aforementioned method is that the experimental transconductance data is never truly linear due to sub-threshold currents and inherent device resistances to name a few. In our method we suggest that one calculates a range of mobilities based on eqn (13) and obtain an overall average value. Or basically one constructs the  $\mu_{\text{eff}}$  vs gate voltage, which can be used to determine the  $D_{it}$  as a function of surface potential as shown in Fig. 1. Averaging over a spread of

mobility values based on the actual gate voltages results in a more accurate description of the mobility. We must emphasize that this method does not currently attempt to determine the interface trap distribution throughout the band gap for which  $C-V$  techniques are still the best methods. What our method allows for, if properly employed, is the rapid determination of an overall average value for the interface trap density given transconductance data (which is generally reported). Our method also allows determination of  $D_{it}$  near the band edges which is quite difficult using other methods.

#### 4. CONCLUSIONS

Our relationship provides a simple means to approximate the interface state density based on transconductance data. Moreover, being a more direct method, the transconductance method enable us to pinpoint the undesirable influence of the interface traps directly on device performance. Although, one must always make assumptions when developing any model relating to device behavior, our method does calculate values comparable to that given in the literature as discussed earlier. It appears that progress is continuing on reducing the problem of interface traps in SiC, although further efforts are needed to reduce them to levels comparable to Si. This shall surely continue as improved fabrication methods are developed.

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