



A RELATIONSHIP BETWEEN INTERFACE TRAP DENSITY AND TRANSCONDUCTANCE IN DEPLETION-MODE FIELD EFFECT TRANSISTORS

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Abstract—A simple relationship between the interface trap densities and transconductance of depletion mode field-effect transistors is derived without any simplifying assumptions regarding the energy distribution of the traps. Using this relationship and the experimental transconductance data, interface trap densities in GaAs and InP were calculated and compared to their values obtained using capacitance versus voltage measurements. Our method provides a simple and efficient technique of estimating interface trap densities based on transconductance data that are readily given in the pertinent literature.

1. INTRODUCTION

Except in silicon, where interface trap densities of SiO₂/Si system are reduced below 10¹⁰ eV⁻¹ cm⁻², field-effect transistors of other semiconductors like GaAs and InP are plagued by the large densities of interface traps, in excess of 10¹¹ eV⁻¹ cm⁻²[1]. This shortcoming, however, is offset by the desirable band structure of these compound semiconductors that enables them to be utilized in light generating and very high speed electronic devices[2].

It is well known that allowed energy states, that usually reside in the forbidden energy gap, are present at the surface of semiconductor crystals[3,4]. The quantum mechanical origins of these states were demonstrated at the early stages of the development of the semiconductor electronics[5,6]. Shockley showed that when finite numbers of atoms are brought together to form a cluster, there exist orbitals with energies residing between the bonding and anti-bonding bands[5]. These orbitals usually are not present when very large numbers of atoms are constituting the crystal. On the other hand, Tamm showed that localized electronic states with energies inside the band-gap exist due to the termination of the periodic structure of the crystals at the surface[6]. Simply stated, the surface states can be viewed as electronic states generated by unsaturated dangling bonds of the surface atoms[3]. In the laboratory environment crystal surfaces are usually covered with layers of native oxides and organic contaminants, and surface

states in the presence of these layers are modified and referred to as "interface states".

While interface traps are undesirable both in minority and majority carrier devices, they can be fatal in some majority carrier devices by pinning the Fermi-level and disabling the field-effect[7-10]. At the time of writing this article, it was not possible to fabricate enhancement mode GaAs metal-insulator-semiconductor field-effect transistors (MISFET) because of the presence of large interface-state densities at the GaAs surface. In the case of depletion mode GaAs MISFETs, as we will show in the next section, interface traps may drastically reduce the transconductance (g_m) of the transistor.

Recently we reported some interesting results regarding the passivation of GaAs using metal-organic chemical vapor deposited (MOCVD) cubic-GaS[11]. We performed extensive optical and electrical measurements to study the effectiveness of cubic-GaS as a passivation layer and as an insulator[11,12]. We also fabricated GaS/GaAs MISFETs with relatively large transconductance of 70 mS/mm[12] (g_m s as high as 150 mS/mm have also been observed).

In an attempt to compare our results with the ones reported in the literature, we discovered that most researchers report either g_m s or D_{it} s, and these are rarely reported simultaneously. There is also a question regarding what levels of D_{it} s are acceptable from the device operation point of view? Finally, we wanted to know how the combination of insulator capacitance, and the channel doping level can be altered to offset the effect of the interface traps on g_m and to obtain a simple design rule regarding these

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parameters. Our motivations in the present study, therefore, are: (i) estimate D_{it} given g_m and vice versa; (ii) determine the importance of the interface traps in reducing g_m ; and (iii) develop simple rules in designing III-V compound semiconductor MISFETs.

Furthermore, one of the interesting and important questions in device modeling, in general, is how device parameters are affected by that of the materials? Using numerical methods it is not very difficult to incorporate material parameters in the equations governing the device behavior and numerical methods are routinely used by most researchers in the field. However, it is almost universally accepted that numerical methods are not effective tools in developing an overall picture and intuition regarding the device behavior. On the other hand, closed form relationships are usually derived using many simplifications that, in some cases, render them ineffective in explaining the device behavior. More often, however, simple closed form analytical relationships help us to develop a mental picture of the underlying processes.

Here we present a simple relationship between the transconductance of the depletion mode field-effect transistor and trap densities at its gate-channel interface. Transconductance and interface trap densities are commonly measured to characterize devices, and are widely reported in the literature. The relationship that is derived in the present work enabled us to make direct comparison between the ideal transconductance and its experimental value taking into account the trap densities.

2. THEORETICAL CONSIDERATIONS

Interface traps, depending on how fast they can trap and release mobile charges, can be divided into slow and fast traps, respectively denoted by D_{its} and D_{itf} . By definition, D_{its} can only respond to very slowly varying signals while D_{itf} can follow both slow and fast signals. Therefore, depending on whether the transconductance is measured using d.c. or a.c. signals, it will be affected differentially by the interface-states.

In r.f. applications, transistors are usually d.c. biased into a quiescent operation point, where they are operated as a.c. amplifiers and other active elements. Slow traps usually affect the bias point of the transistor causing it to shift as a function of time, while they do not affect the a.c. response of the transistor. Fast traps, on the other hand, being able to follow both d.c. biases and a.c. signals, contribute to the initial quiescent operation point and to the a.c. characteristics of the transistor. They do not, however, affect the quiescent operation point as a function of time.

In switching applications, transistors are pushed from "off" states to "on" states by applying appropriate signal steps. Both fast and slow traps affect the switching behavior of the FET.

In ideal MISFETs, the a.c. and d.c. transconductances are related to each other through a relatively simple feed-back relationship; their switching behavior is determined by carrier transit time and various charging time constants. In the presence of slow and fast interface traps, the a.c. and d.c. transconductances should be examined individually. Here, we only discuss the d.c. case. The a.c. and switching behaviors of FETs will be discussed in a future publication.

2.1. D.C. relationship

In a metal-insulator-semiconductor structure [13] (Fig. 1) the gate voltage (V_g) is the sum of the insulator voltage (V_i), and the semiconductor surface potential (ψ_s). Furthermore, V_i is

$$\frac{Q_{sc}}{C_i},$$

where C_i is the insulator capacitance (per unit area) and Q_{sc} is the semiconductor space charge ($Q_{sc} = \sqrt{2qN\epsilon_s\psi_s}$, where N is the doping density, q is the electronic charge, and ϵ_s is the permittivity of the semiconductor).

To analyze the performance of real devices, three parameters should be taken into account: (i) the effect of the distance between gate and source; (ii) fast and slow interface traps and fixed gate insulator charges; and (iii) non-zero work function difference between the gate metal and the semiconductor (taken to be zero in the present work). The non-zero gate and source distance results in a resistance between the source and the channel under the gate (R_{SG}) that reduces the magnitude of the measured transconductance. On the other hand, interface-states trap charges resulting in an additional voltage drop across the insulator (V_{it}). The gate voltage applied through the external gate contact (V'_g) is given by:

$$V'_g = V_g + V_{it} + R_{SG} I_{DS}. \quad (1)$$

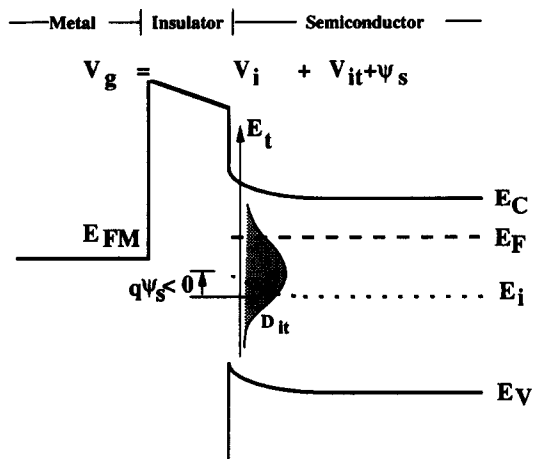


Fig. 1. Metal-insulator-semiconductor structure. The surface potential (ψ_s) by definition is negative for depleted n -type semiconductor surface.

Assuming that there are no fixed oxide charges, V_{it} is related to the charges (Q_{it}) that are trapped at the interface states:

$$V_{it} = \frac{Q_{it}}{C_i}. \quad (2)$$

Q_{it} is related to the total interface trap density (D_{it}):

$$Q_{it}(\psi_s) = q \int_{E_v}^{E_F + q\psi_s} D_{it}(E) dE, \quad (3)$$

where $D_{it} = D_{its} + D_{itf}$. In the above equation it is assumed that the slow traps have reached the equilibrium. As mentioned before, this assumption may not be valid resulting in the charge occupancy of the slow traps to change as a function of time and making Q_{it} time dependent.

Transconductance is usually measured at a fixed drain voltage by incrementing the gate voltage and measuring the resulting increment in the drain current:

$$g'_m = \left. \frac{\partial I_{DS}}{\partial V'_g} \right|_{V_{DS} = \text{const}},$$

where V'_g is the externally applied gate bias. The theoretical transconductance g_m , on the other hand, is given by:

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_g} \right|_{V_{DS} = \text{const}},$$

where V_g is the bias appearing between the gate and the channel. Differentiating eqn (4) with respect to I_{DS} and noting that V_{it} is a function of ψ_s we get:

$$\frac{\partial V'_g}{\partial I_{DS}} = \frac{\partial V_g}{\partial I_{DS}} + \frac{\partial V_{it}}{\partial q\psi_s} \frac{\partial q\psi_s}{\partial V_g} \frac{\partial V_g}{\partial I_{DS}} + R_{SG}. \quad (4)$$

Using the definition of g_m and g'_m , eqn (4) can be re-written as:

$$g_m^{-1} = g_m^{-1} + \frac{\partial V_{it}}{\partial q\psi_s} \frac{\partial q\psi_s}{\partial V_g} g_m^{-1} + R_{SG}. \quad (5)$$

The term involving V_{it} in eqn (5) can be evaluated using eqns (2) and (3) yielding the following relationship between D_{it} and the d.c. transconductance:

$$\begin{aligned} g_m^{-1} &= g_m^{-1} + \frac{qD_{it}(E_F + q\psi_s)}{C_i} \\ &\times \left(\frac{q}{1 + (\sqrt{-q\epsilon_s N_D / 2\psi_s}) / C_i} \right) g_m^{-1} \\ &+ R_{SG}. \quad (\psi_s < 0) \end{aligned} \quad (6)$$

With R_{SG} set equal to zero we define an ideality factor η as follows:

$$\begin{aligned} \eta &= \frac{g'_m}{g_m} \\ &= \left(1 + \frac{q^2 D_{it}(E_F + q\psi_s) / C_i}{(\sqrt{-q\epsilon_s N_D / 2\psi_s}) / C_i + 1} \right)^{-1}. \quad (\psi_s < 0) \end{aligned} \quad (7)$$

In eqn (7), D_{it} is the sum of fast and slow traps. Fast traps are at equilibrium with the d.c. bias, while

the slow traps may not be at equilibrium. This will cause η to change as a function of time. It should be emphasized that N_D (the doping density) in eqn (7) is assumed to be uniform throughout the channel. Equation (7) can be written by taking the energy of the interface states (E_{it}) as the independent variable ($E_{it} = E_F + \psi_s$) or, alternately, by taking the gate voltage as the independent variable.

The form of eqn (7) is very revealing since it clearly shows that as D_{it} is made larger the experimentally measured transconductance becomes smaller. Moreover, it suggests that by making N_D and C_i larger, one can oppose the effect of the D_{it} on the transconductance. Surprisingly, at flat-band ($\psi_s = 0$) the experimental and ideal transconductances are equal. We will discuss the effect of the interface traps in a.c. measurements in a future publication. However, it is interesting to note that the definition of the ideality factor η also simplifies the a.c. analysis. Equation (7) indicates that at any given frequency, η will only be affected by those traps that can respond at that frequency. Due to the distribution of traps over energies, however, a single cut-off frequency cannot be defined and the cut-off frequency is a function of the trap energy.

Usually two types of interface trap densities are reported in the literature which are shown in Fig. 2(a) as type "A" and type "B" distributions. Both types of trap densities increase rapidly near the band edges and type B [Fig. 2(a)] has traps with a Gaussian distribution around the mid-gap energies.

Using eqn (7) and interface trap densities shown in Fig. 2(a), we calculated η versus the gate voltage for a GaS/GaAs MISFET structure. The device parameters used in calculation of η are shown in Table 1 and they are identical to parameters of a GaS/GaAs MISFET that was fabricated and reported previously[12]. Figure 2(b) shows the η versus the gate voltage for the two types of D_{it} s. When the gate voltage is small, the capacitance due to the space charge region is very large, masking the contribution of the interface traps to the transconductance. As the gate bias increases, the space charge capacitance decreases and the interface traps become important and affect the ideality factor. The interesting feature in Fig. 2(b) is that the mid-gap interface states in type B distribution directly reduce the ideality factor. Near the valence band edge, the interface trap densities increase, diminishing the ideality factor for larger depleting gate voltages.

3. EXPERIMENTAL DATA

To examine the usefulness of eqn (7), we conducted a series of experiments using GaS/GaAs MISFETs. We measured their gate-to-source high frequency (using Keithley 590) and quasi-static (using Keithley 595) $C-V$ and calculated interface trap densities as a function of energy and gate voltage. Furthermore, using a parameter analyzer (HP 4145B), we also

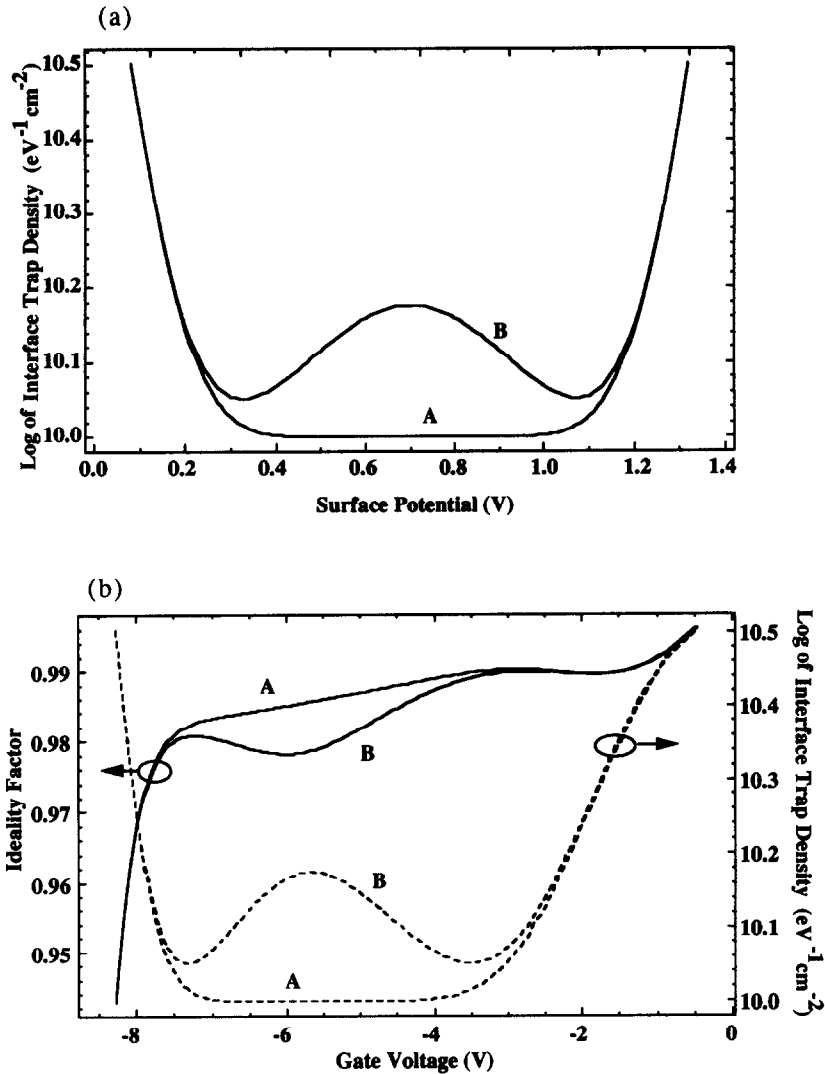


Fig. 2. (a) Two types of interface trap distributions (D_{it}) that are commonly observed in semiconductors. (b) Calculated ideality factors (η) versus the surface potential in an N -channel depletion mode GaAs metal-insulator-semiconductor field-effect transistor with type A and type B interface trap densities.

Table 1. Device parameters used in calculating interface trap densities shown in Figs 2-5

Device Parameter	Gas/GaAs MISFET	Anodic oxide/GaAs MISFET	$\text{Si}_3\text{N}_4/\text{Si}/\text{Ge}/\text{GaAs}$ MISFET
Doping (cm^{-3})	$N_d \approx 4 \times 10^{16}$	$N_d \approx 1 \times 10^7$	$N_d \approx 2 \times 10^{17}$
Mobility ($\text{V}/\text{cm}^2 \cdot \text{s}$)	4600	2000	~ 2000
Gate insulator (\AA)	300	1000	150/10/20
Channel length (μm)	5	4	3
Channel width (μm)	100	260	145
Channel depth (μm)	0.5	0.19	0.1
Flat-band voltage (V)	1	-2	0.5
Pinch-off voltage (V)	-6	-3.5	-4.5
Reference	[8]	[4]	[10]

measured the transconductance of these devices as a function of the gate voltage. Gate areas along with high frequency $1/C^2$ versus voltage measurements were then used to determine the channel doping. Using the doping level and drain to source current measurements we estimated the channel mobility. Table 1 summarizes these experimentally determined device parameters.

Next we calculated the theoretical transconductance versus gate voltage of the above devices using the following relationship that is valid for long gate length depletion mode transistors in saturation:

$$g_m = \frac{qN\mu aZ}{L} \left(1 - \sqrt{\frac{V_g + V_{bi}}{V_p}} \right), \quad (8)$$

where N is the doping density (assuming all ionized), μ is the carrier mobility, a is the channel depth (epitaxial layer thickness), Z is the channel width, L is the channel length, V_{bi} is the built-in potential

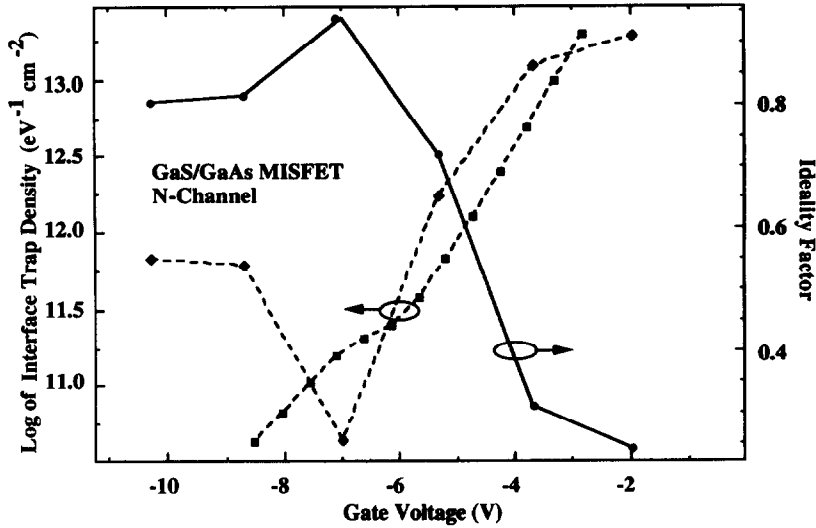


Fig. 3. D_{it} and η as a function of the surface potential and gate voltage of a GaS/GaAs metal-insulator-semiconductor field-effect transistor (MISFET) calculated from capacitance versus voltage data reported in Ref. [11] and the MISFET transconductance data reported in Ref. [12].

accounting for the surface potential at zero gate voltage, and V_p is the channel pinch-off voltage. The ideality factor for each transistor was then calculated by taking the ratio between the experimental and the theoretical transconductances.

In cases where R_{SG} s were large, we took it into account and calculated a corrected experimental transconductance (g'_m) given by $g''_m/(1 - R_{SG}g''_m)$, where g''_m is the measured transconductance.

Figure 3 shows the ideality factor and interface trap density as a function of gate voltage of a GaS/GaAs MISFET. We have reported the fabrication and transistor characteristics of GaS/GaAs MISFET elsewhere[12] and its parameters are shown in Table 1. The agreement between the interface trap

densities determined using $C-V$ measurements[11] and eqn (10) is quite satisfactory.

In Figure 4 we show the ideality factor and the resulting interface trap density that we calculated for an anodic oxide/GaAs transistor that is reported in Ref. [14] (its parameters are given in Table 1). In Fig. 4, D_{it} extends over a range of two orders of magnitude from $10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ up to $10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$. Since $C-V$ data was not given for this transistor, we could not include the corresponding D_{it} curve.

Figure 5 shows the $D_{it}-V_g$ curve of an $\text{Si}_3\text{N}_4/\text{Si}/\text{Ge}/\text{GaAs}$ transistor that was calculated using the transconductance data reported in Ref. [14]. The reported D_{it} for this transistor, that was calculated using the conductance measurement, was

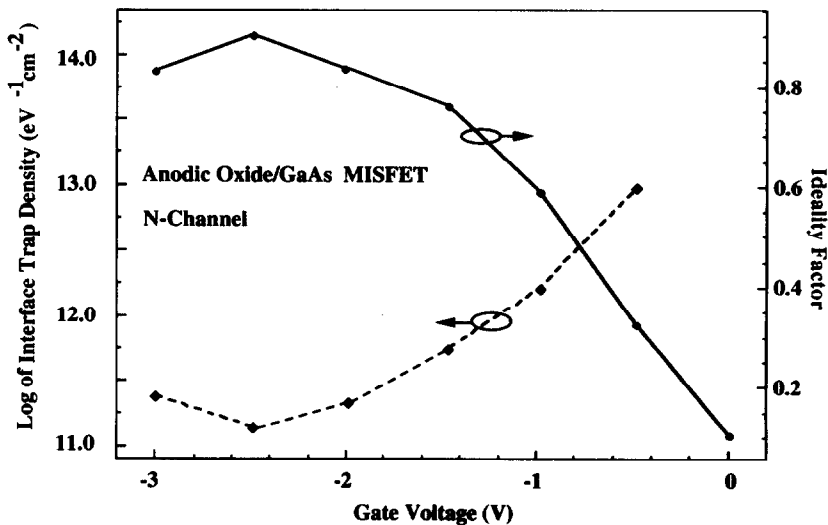


Fig. 4. D_{it} and η as a function of the surface potential and the gate voltage of an anodic oxide/GaAs MISFET calculated using the transconductance versus voltage measurements reported in Ref. [10].

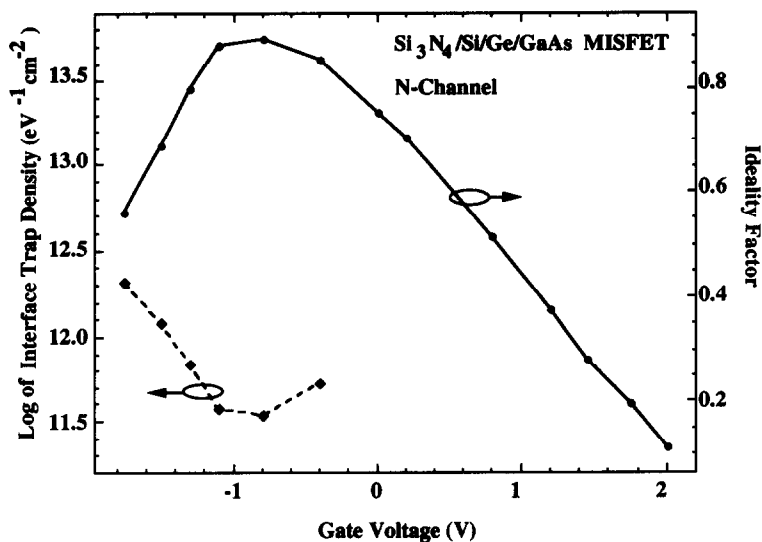


Fig. 5. D_{it} and η as a function of the surface potential and the gate voltage of an $\text{Si}_3\text{N}_4/\text{Si}/\text{Ge}/\text{GaAs}$ MISFET calculated using the transconductance versus voltage measurements reported in Ref. [14].

$2 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ [14] which agrees with the minimum D_{it} in Fig. 5. In calculating the ideal transconductance for this transistor we assumed a channel electron mobility of $2000 \text{ cm}^2/\text{V}\cdot\text{s}$ (this was not reported in Ref. [14]) and the transistor width was taken to be $145 \mu\text{m}$ [14,15].

4. CONCLUSION

We derived a simple relationship between the d.c. transconductance and interface trap density in depletion-mode field effect transistors. Since transconductance data are more routinely reported in the literature than interface trap densities, our relationship enabled us to compare interface trap densities in a variety of devices. It also enabled us to estimate the effectiveness of passivation of GaAs using different methods (cubic-GaS and Si_3N_4). The form of the relationship was also very revealing and it clearly showed how the doping density and the device geometry can be varied to oppose the effect of interface traps on the transconductance of the device.

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