

NONDESTRUCTIVE EVALUATION OF GENERATION LIFETIME AND SURFACE GENERATION VELOCITY AND THE EFFECT OF ETCHING, POLISHING AND ANNEALING ON 5" Si WAFER SURFACE PROPERTIES

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ABSTRACT

In this work the nondestructive measurements of bulk generation lifetime, τ_g and surface generation velocity S_g are discussed and experimentally demonstrated. The technique is based on transverse acoustoelectric voltage (TAV) transient measurements. τ_g and S_g are evaluated to characterize the electrical properties of Si wafers prior to the device fabrication. The wafers have undergone different chemical etch removal, polish removal and forming gas annealing treatments. Measurements under the applied DC electric field are performed in order to distinguish between the surface and bulk effects. The results indicate: 1) Increase of the effective lifetime, τ_{eff} by about 100 times after etching and polishing due to the surface damage removal, 2) A minimum of two orders of magnitude improvement is observed for the forming gas annealed half wafers as compared to the unannealed halves. In the above experiments both oxidized and unoxidized samples are investigated without the fabrication of any form of contact on the wafers. The spatial maps of τ_g and S_g are obtained for some wafers. The TAV amplitude and time constant dependence on the applied DC voltage reveals the surface condition (depletion or inversion) at zero bias and the approximate position of the recombination center within the Si bandgap.

INTRODUCTION

Increasing levels of integration and larger chip area of VLSI circuits demand a high level of automation for IC fabrication processes. One area of great importance is the testing of wafer parameters after fabrication steps. Nondestructive testing methods are of growing interest due to their possible application in automated production lines. In this work the electrical properties of 5" silicon wafers which have undergone different etching and polishing removals are monitored non-destructively.

After the silicon wafers are sliced from the ingot by inner diameter slicing and edge rounded, they undergo etching and polishing steps before device

fabrication processes (1). Chemical etching step is used to remove the damage and contamination which is left from the slicing process. The chemical etch removal is typically about one mil per side. After etching the polishing step is performed to obtain the necessary flatness, specular surface, lack of features, and parallel surfaces of the wafer. In addition, polishing should not introduce any damage or contamination to the surface. Typical polish removal is on the order of a fraction of a mil. The extensive use of chemical etching followed by polishing is due to the fast removal rate by etching (economical, high throughput) and the required optical properties which can only be obtained by polishing (slow process). The extent of the damage removal by the above steps are monitored by measuring the generation lifetime, τ_g and surface generation velocity, S_g since these parameters are dependent on the magnitude of the surface damage and defect density. τ_g and S_g are also used to investigate the effectiveness of the forming gas annealing process on the reduction of the interface states density for 3" silicon wafers. The evaluation of the effective lifetime, τ_{eff} which is approximately related to τ_g and S_g by the following equation:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_g} + \frac{S_g}{L_D} \quad \text{near flat band condition} \quad (1)$$

where L_D is the extrinsic Debye length, is discussed elsewhere (2). The separation of τ_g and S_g is possible by the application of a depleting DC bias field across the semiconductor. Under bias, L_D is replaced by the depletion layer thickness W which can be modulated to a maximum value determined by the onset of inversion (3). If a DC bias field is used, the maximum depletion width, W_m is on the order of 0.5 μm for $\rho = 11\text{-}16\Omega\text{ cm}$ silicon. Pulsed bias field should be used in the following conditions: 1) if the silicon wafer exhibits a large surface generation velocity and 2) in the case of depth profiling of τ_g to the distances larger than W_m . Using the pulsed bias field, the experimental setup should be capable of measuring τ_g in time scales much shorter than the minority carrier build-up time in the depletion region (storage time).

The dependence of τ_{eff} and TAV amplitude on the applied bias field reveal the surface condition and the approximate energy level of the recombination center within silicon bandgap (4). The spatial

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maps of τ_g and S_g for some of the samples are presented and the results are compared.

EXPERIMENTAL PROCEDURE

Nondestructive measurement using transverse acoustoelectric voltage (TAV) is described in detail elsewhere (2,3). The measurement is simply done by placing the silicon wafers on the top of a piezoelectric material (LiNbO_3). There is an Al structure evaporated on the surface of the LiNbO_3 with an interaction window at the center of this structure (3). At the interaction region, the electric field (which is perpendicular to the surface of the piezoelectric material) interacts nonlinearly with the near surface free carriers and the TAV is generated across the wafer. The TAV signal is monitored via an Al plate which is pressed on the back side of the wafer and the Al structure on the surface of the piezoelectric material (ground path). Both the TAV amplitude and transient time constants are measured at zero bias field and under applied DC bias to characterize the wafer surface properties.

To evaluate the damage removal properties of etching and polishing, a total number of ten 5" silicon wafers are prepared. All the wafers are sliced from cz grown, p type, $\rho = 11\text{-}16\Omega\text{ cm}$, (100) surface silicon ingots and have undergone different etching and polishing times. Acid etching is used and the etchant mixture is 5:2:1 volume ratio of $\text{HNO}_3/\text{HF}/\text{H}_2\text{O}_2$. Etching is at room temperature and the etching barrel and wafer holder rotate during the process. For polishing, SiO_2 based slurries are used in the simultaneous two sided polishing arrangement. The silicon removal for the wafers reported in this work (measured by capacitive probing) are as follows:

Wafer #	Chem. Etch Removal Both Sides (mils)	Polish Removal Both Sides (mils)	Total Removal Both Sides (mils)
14	0	0	0
13	0.4	0	0.4
16	7.2	0	7.2
10	0.4	2.2	2.6

After etching and polishing the samples are annealed in N_2 ambient at 1000°C followed by another annealing in forming gas (5-10% H_2 in N_2) at 400°C for about 20 minutes. Prior to the measurements the wafers are cleaned in 8 steps, starting with the sulfuric/nitric acid organic material remover followed by immersion in acidic and basic hydrogen peroxide solutions in order to remove metallic contamination and ionic charges.

To investigate the forming gas annealing effectiveness, five 3" silicon wafers are oxidized, annealed, cleaved and then random halves are annealed again in forming gas. The oxidation is dry-wet-dry and the oxide thickness is $550 \pm 50\text{ nm}$. Post oxidation annealing is performed in N_2 at 1000°C to reduce the oxide fixed charges. Forming gas (F.G.) annealing is as described before and is done to reduce the interface states density. τ_{eff}

is measured using TAV waveform and the results are compared for no F.G. and F.G. annealed wafer halves.

RESULTS AND DISCUSSION

The time constant associated with the TAV transients (τ_{eff}) is related to τ_g and S_g as shown in equation 1 (2). The experimental results for differently etched and polished wafers are presented in figure 1. τ_{eff} (at zero bias) is plotted as a function of position for different wafers. The plots indicate a large spatial variation of τ_{eff} for each wafer with generally lower values towards the edge. This can be due to the handling damage around the wafer edges. It is shown (figure 1) that by chemical etching the lifetime increases which is an indication of surface damage removed. Sample #16 (7.1 mils etching removal) exhibits about 10^2 times increase in the lifetime as compared to as sliced sample (#14). The wafer which is both etched and polished (#10) exhibits a longer average lifetime than the wafer which is only etched (#16) even though the total removal is less. This result might indicate that polishing is to some extent, more effective than chemical etching in producing a damage free surface. The argument is not conclusive and more experimental data is needed. One reason is that #10 and 16 wafers might not be the successive slices from the same ingot which can easily cause a twofold variation in lifetime even if the wafers undergo the same etching and polishing. This effect is verified experimentally.

In order to determine the contributions of τ_g and S_g to the measured effective lifetime, the measurements under the applied depleting voltage are performed. The results for as sliced sample (#14) is in the form of spatial variations of τ_g and S_g and is shown in figure 2. The depleting DC bias voltage is chosen at a value corresponding to the maximum measurable lifetime before the onset of inversion. The reason is to quench the surface effect as much as possible by going further into the bulk. The measured lifetime under the applied voltage is approximately the bulk generation lifetime (the contribution of the diffusion current is neglected). The variations of τ_g and S_g indicate that the increase of S_g towards the wafer edges is dominantly responsible for lower τ_{eff} close to the wafer periphery and the bulk generation lifetime varies slightly across the wafer.

The TAV amplitude and τ_{eff} dependence on the applied DC voltage (TAV-V and τ -V) for wafer #16 are shown in figure 3. The forms of the plots are more or less the same for other samples with a difference only in the TAV and τ absolute values. It should be noted that the polarity of the applied DC voltage is opposite as compared to the gate bias in C-V measurements (2,3). Thus the negative applied voltage tends to deplete and invert the surface. The τ -V curve shows an increase of the τ_{eff} for higher depleting voltages and a maximum in the positive applied voltage direction is observed. In order to determine the surface potential at different bias voltages, the TAV-V curve is used. By comparing the TAV-V plot to the theoretical curve in reference (3), the surface potential can be approximated to be about 0.23V at zero bias

(point A) and about 0.15V at $V_{\text{appl.}} = +0.5\text{V}$ which corresponds to the maximum in the τ -V curve (point B). Figure 4 shows the energy band diagram and the approximate band bendings corresponding to the points A and B (notice the surface depletion at zero bias). In order to explain the τ -V curve, two superimposing phenomena are considered: 1) the increase of the depleting bias field (negative values) increases the τ_{eff} due to the larger depletion width which reduces the surface effect, 2) the presence of the recombination center at the energy level, E_T which is at 0.15 eV from the intrinsic energy level, E_i produces the maximum in the τ -V curve (4,5). The reason is attributed to the maximum τ_g which is obtained upon the passage of E_T through the fermi level ($E_T(B) = E_f$, point B).

The effect of forming gas annealing on the τ_{eff} is demonstrated in the following table:

	τ_{eff} (μsec) @ zero bias voltage				
Sample #	1	2	3	4	5
No F.G.	2	100	1	1	1
F.G.	620	1600	120	500	220

Table 1. Comparison between No F.G. and F.G. annealed half wafers

Table 1 shows an average increase of the τ_{eff} in the order of 230 times for the forming gas annealed half wafers.

The values of τ_{eff} for samples which are sliced from different section of an ingot and are etched similarly (total removal of 5 mils) are shown in Table 2.

τ_{eff} (μsec) @ zero bias voltage		
Seed	middle	Tail
440	239	203

Table 2. Comparison between different sections of the ingot.

The results indicate a lower surface damage for the seed part as compared to the tail and middle sections.

CONCLUSION

The presented experimental results show that the nondestructive transverse acoustoelectric voltage measurement is indeed a feasible technique to characterize the silicon wafer electrical properties under any kind of surface condition. The application of DC bias voltage to distinguish between τ_g and S_g which was proposed previously (2) is experimentally demonstrated in this work. Monitoring τ_{eff} , τ_g and S_g for silicon wafers which have undergone different etching and polishing steps reveals the extent of the effectiveness of these steps in producing a damage free surface. The effect of forming gas annealing in reducing

the interface states density is also demonstrated. In all the above experiments no contact of any form is fabricated on the silicon surface and the presence or absence of the insulator layer is immaterial.

Automated equipment is being developed where up to 256 x 256 points on the wafer can be evaluated with respect to parameters such as τ_g and S_g . The final objective of the equipment will be to present the results in the form of images in pseudo-color where each color represents a certain range of the above parameters.

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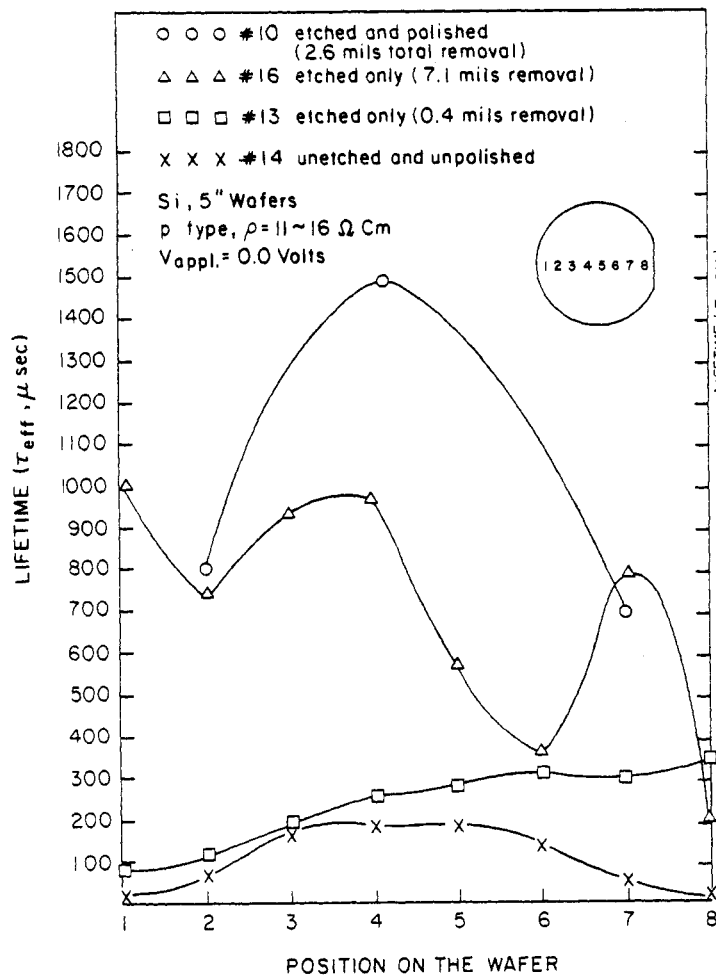


Figure 1. Spatial variation of τ_{eff} for silicon wafers

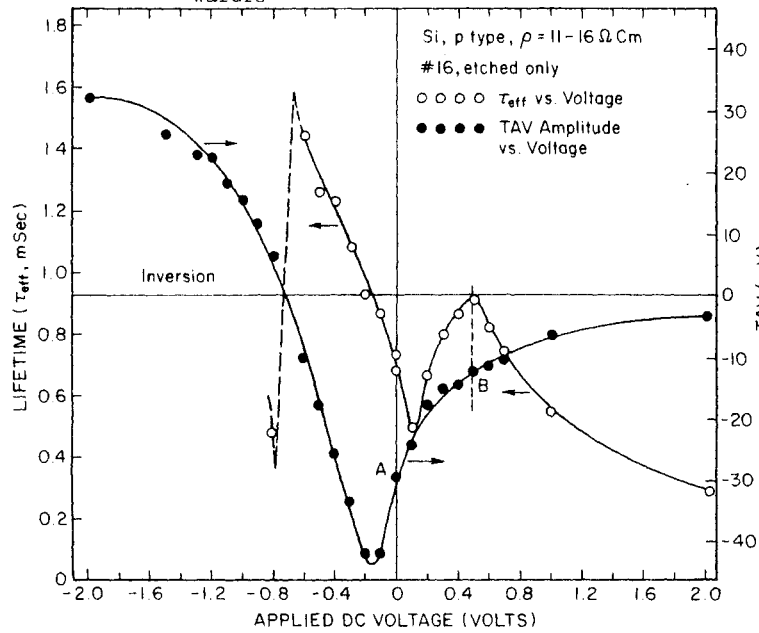


Figure 3. TAV and τ_{eff} dependence on the applied bias voltage for etched silicon wafer

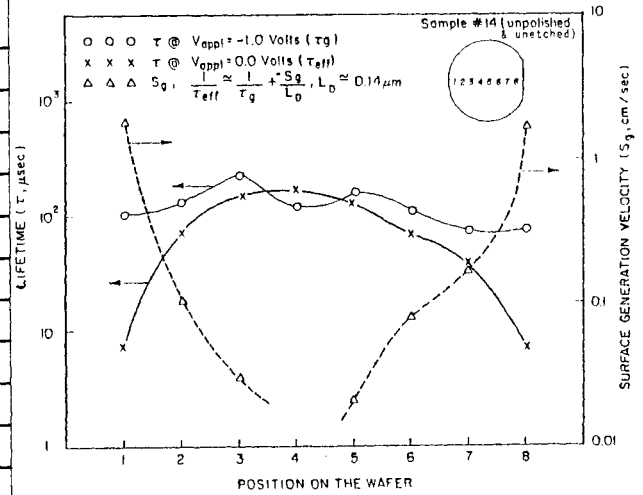


Figure 2. Spatial variation of τ_g and S_g for as sliced Si wafer

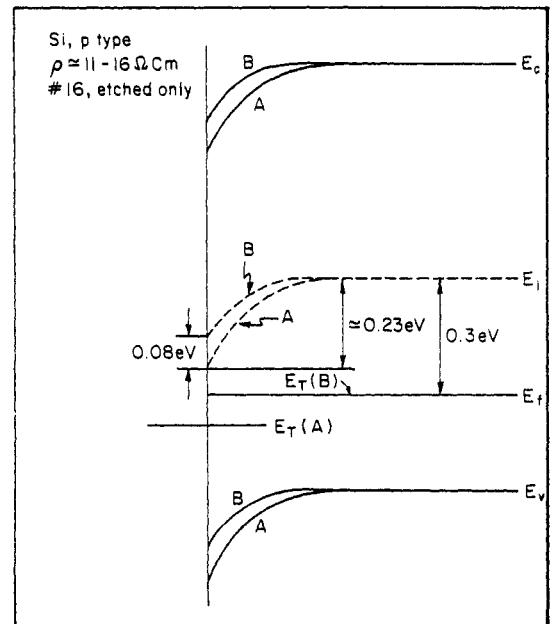


Figure 4. Energy band diagram corresponding to the data presented in figure 3