

Ultralow-Power Adaptive System Architecture Using Complementary Nano-Electromechanical Carbon Nanotube Switches

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Abstract

As an alternative to conventional CMOS devices, we propose a new family of devices called “Complementary Nano Electro-Mechanical Switches” (CNEMS) using carbon nanotubes as active switching/latching elements. The basic structure of these devices consists of three co-planar carbon nanotubes arranged so that the central nanotube can touch the two side carbon nanotubes upon application of a voltage pulse between them. Owing to the unique properties of carbon nanotubes, these devices have very low leakage current, low operation voltages, and built-in energy storage to reduce computation power, resulting in very low overall power dissipation. Besides, these devices have latching mechanism for non-volatile memory-mode operation. The devices can also be readily integrated in the same substrate as CMOS transistors allowing easy manufacturability and hybridization with conventional CMOS devices. System design using CNEMS devices, however, brings in new set of challenges. Based on our analysis of CNEMS devices we have fabricated, in this paper, we propose circuit implementation styles and an architectural framework for digital system design using these devices. The architecture can dynamically adapt to application workload for optimized performance and reconfigure around defects / variations for reliable operation.

1. Introduction

While CMOS technology has served the industry marvelously so far (by allowing nearly exponential growth in performance and device integration density), it is predicted to meet the end of roadmap soon in near future due to the intrinsic physical limitations of the device in terms of scalability. At nanometer scale, CMOS devices suffer from increasing short channel effect that results in high leakage current and contributes to large wasted power. Along with leakage power, dynamic power has also increased significantly with increasing clock rate and more number of devices on die. Consequently, high average power and power density have emerged as major barriers to gigascale integration. On the other hand, drain to source voltage

(V_{DS}) reduces with scaling, while the series resistance increases, giving rise to reduced saturation current and I_{ON}/I_{OFF} ratio. Variations in manufacturing process parameters, such as length (L), width (W), threshold voltage (V_{TH}) have increased alarmingly [14] with continued miniaturization of device geometry and supply/threshold voltage scaling. Hence, manufacturing yield and robustness of operation under severe process variations have manifested as major concerns to the designers of digital systems at nanometer scale. To address these issues, there has been multitude of efforts to develop alternative devices with promising characteristics in terms of performance and/or integration density. Most of these emerging devices have either prohibitive manufacturing costs or they introduce a completely new paradigm of computing. However, to achieve a smooth transition from conventional MOSFET devices to a viable alternative at the end its roadmap, we need a potent technology, which allows system manufacturing by extending the existing CMOS fabrication and enables utilization of the rich repository of existing CAD tools.

In this paper, we consider a new device that uses carbon nanotube (CNT) [1, 3] as active element to develop a Complementary Nano Electro-Mechanical Switch, referred as CNEMS. Acting as a mechanical relay, the switch (described in details in the Section 2) can be toggled between two complementary configurations by application of an electric field between two of its terminals. Once configured in a certain way, the switch remains in the same state until an opposite electric field is applied to reconfigure the switch. Due to this latching mechanism, *each switch works as a non-volatile memory element*. In a CNEMS, electron transport between two connected terminals is ballistic. Due to the electro-mechanical nature of the switch, there is virtually no leakage current between two terminals when they are not connected. Another important feature of the device is that, once it is programmed, certain amount of elastic energy remains internally stored in the carbon nanotubes, so that all subsequent reconfigurations of the switch require less electric field and thus less energy for transition. *This feature of internal energy storage [6, 7] helps to reduce the active power of the switch considerably.*

Owing to the unique properties of carbon nanotubes, these devices have very low leakage and low operation voltage. Since the CNEMS has low leakage, it has extremely high data retention capability. The device is also completely immune to soft error (e.g. memory failures due to alpha/neutron particle hit) [17], unlike CMOS based memory. Therefore, along with its ability for Ultra Large Scale Integration (ULSI) [4, 18], CNEMS is a good candidate for memory implementation and can potentially replace conventional charge-based CMOS static and dynamic RAM. Unlike the conventional CMOS logic circuits, which evaluates logic function based on charge stored in a node [13] (defined by the diffusion and or gate capacitances of the devices), the proposed CNEMS based logic evaluates in two steps: a) configure and then b) evaluate. In the “configure” step, the switch is programmed to select one of the two inputs and in the following “evaluate” step, the switch propagates the right input signal to the output. The proposed switch has high noise margin with stable on and off state. Moreover, due to the complementary nature of the switch, special logic structure such as decoder etc. can be realized with it in a very efficient way.

In this paper, we analyze the device properties (Section 2) and propose circuit/architecture implementation with these devices. In particular, we propose look-up table (LUT) based logic design (Section 3.1), a memory array implementation (Section 3.2) and a reconfigurable architecture (Section 4) that can dynamically adapt to specific applications and defects. We conclude in Section 5.

2. Device and Technology

The electronic switches used in complementary metal-oxide semiconductor field effect transistor integrated circuits (CMOS-IC) dissipate energy due to transition from “on” to “off” states and due to leakage current. The dissipation of energy increases nearly

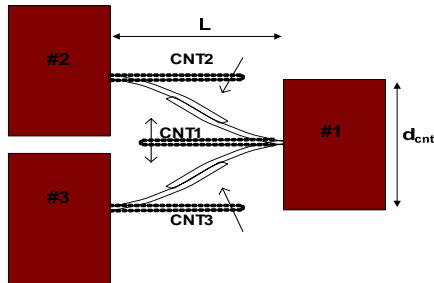


Figure 1. Complementary nano electro-mechanical switch (CNEMS). The central CNT (CNT1) is either touching the top (CNT2) or bottom (CNT3) carbon nanotube. The latching is caused by the van der Waals force and the energy stored in CNT1 is recovered when it is transitioned.

exponentially as these devices are scaled below 60nm gate length. We propose carbon nanotube [1-5] based mechanical switches with internal energy storage to complement and/or an alternative to the existing CMOS switches in certain applications. Devices with internal energy storage were proposed by Feynman [6, 7] and Bennett [8, 9] for reduced power computation and bit processing. The main idea was that if one uses a spring as the computation device, the “one” state may be achieved by compressing the spring and latching it so that it does not spring back. Subsequently, in transitioning to the “zero” state, the stored energy in the compressed spring can be retrieved and re-used to reduce the energy per bit. With the discovery of carbon nanotubes and their applications in electronics [1-5, 10-12, 18], we note that CNTs with their large Young’s modulus (1.3 TPa) [10] and very small diameters (1-100nm), are ideal electronic device-grade “springs” for Feynman-Bennett type computation devices. Hence, we propose to develop a very unique category of electronic devices with internal energy storage capacity and other desirable characteristics such as very low leakage and high transition speeds. The basic structure of the proposed complementary nano electro-mechanical switch consists of three co-planar carbon nanotubes arranged so that the central nanotube can touch the two side carbon nanotubes upon application of a voltage pulse between them. When the central CNT touches one of the side CNTs, the van der Waals force causes them to “stick” to each other resulting in latching. The CNTs are then “unstuck” by applying a voltage between the central CNT and the third CNT on the opposite side. Certain amount of energy is stored in the elastic deformation of the CNT when it is bent to make contact with a side CNT. This energy becomes available when the central CNT is released and attracted to the opposite CNT. Noting that CNTs have very large Young’s modulus of around 1.3 TPa, very fast CNEMS with sub-nanoseconds switching times can be realized provided that CNT lengths are kept below $L < 100\text{nm}$ that in turn requires precise CNT-CNT distances of around $d_{\text{cnt}} < 50\text{nm}$. The proposed CNEMS have very large on-to-off conductance ratio ($> 10^{12}$), are radiation hard, and can be fabricated on CMOS circuits.

2.1. Device Characteristics

CNEMS characteristics critically depends on the kind of carbon nanotube we use, how close we place them near each other and the bottom electrode, and how long the carbon nanotubes are. As discussed next, carbon nanotubes can be single-walled (SWCNT) or multi-walled (MWCNT) depending on how they are grown and their growth temperature. The MWCNTs are usually metallic while SWCNTs can be both

metallic and semiconducting. The gap distance between CNTs and a bottom electrode can be designed to be between 20-100nm. Smaller gaps will result in unwanted van der Waals clamping of the CNTs to the bottom surface while larger gaps will result in unacceptably larger “reset” voltage (V_r = reset voltage is the voltage needed to “un-stuck” all the CNTs from each other so that complete isolation can be achieved between different parts of the circuit.) It is desirable to have the CNT-CNT distance as small as possible because then the threshold voltage (V_{th} = voltage needed to attract adjacent CNTs together) can be made very small and the CNT length can be scaled down correspondingly increasing the transition speed (v_t). We discuss these parameters in detail below.

2.2 Device Operation Principles

To calculate the turn-on, or the threshold, voltage we note that the total energy of two adjacent CNTs is given by $E_t = E_{vdW} + E_{elastic} + E_{electrostatic}$. The van der Waals interaction between CNTs has been calculated by researchers and lower bound to the expected attractive energy can be described using an empirical formula as given below:

$$E_{vdW} = (-0.053 + 0.086d)L \text{ eV, where "d" is the}$$

CNT diameter expressed in \AA and L is the interaction length also in \AA . This empirical equation is only applicable when the CNTs are touching each other. When they are not, Leonard-Jones type of potentials that contain r^{-6} and r^{-12} CNT-CNT position (r) dependences can be used to calculate E_{vdW} as a function of distance. The elastic energy can be calculated using beam mechanics model and is given by:

$$E_{elastic} \sim 1.6 \frac{\delta^2 EI}{L^3} \text{ where } \delta \text{ is the displacement of}$$

CNT's tip, E is the Young's modulus (~ 1.3 TPa for

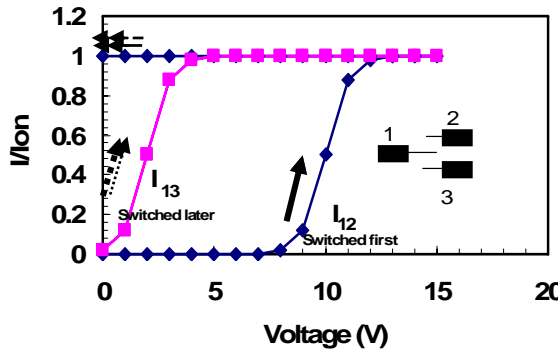


Figure 2. Simulated Switching characteristics of CNEMS ($L \sim 50\text{nm}$, $d_1 \sim 3.5\text{nm}$, $d_2 \sim 3\text{nm}$, and $d_{cnt} \sim 20\text{nm}$, and $\delta \sim 10\text{nm}$).

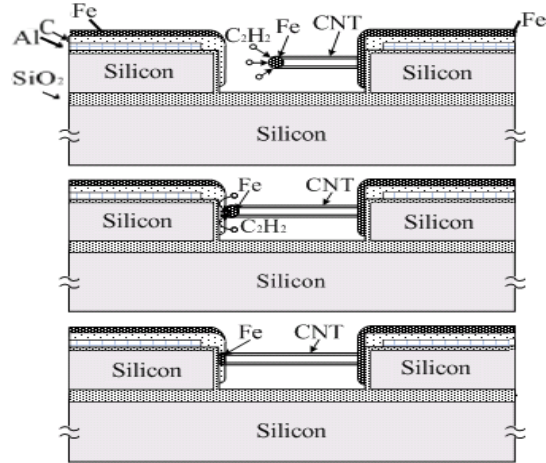


Figure 3. Schematic of the metal-catalyzed chemical vapor deposition of CNT growth mechanism. A thin (5-10nm) layer of iron was used to catalyze the CNT growth. C_2H_2 used as the carbon-providing gas is decomposed to carbon and hydrogen atoms over the iron. The carbon atoms are then dissolved in iron nanoparticles that are formed when the thin layer of iron is broken up in the argon/ C_2H_2 gas flow at 600-700 °C. After carbon concentration reaches saturation levels, CNTs start growing.

SWCNTs), and I is the moment of inertia

$$\left(= \frac{\pi}{64} [d_1^4 - d_2^4] \right), \text{ where } d_1 \text{ is the outer diameter of}$$

the CNT and d_2 is its inner diameter). The electrostatic

$$\text{energy is given by } E_{electrostatic} = \frac{1}{2} CV^2 \text{ where } C \text{ is}$$

the capacitance between two adjacent CNTs and V is the applied voltage. Considering two CNT's symmetrically bending toward each other, the “C” can be approximated using a parallel cylinder capacitor with uniform distance d_{cnt} . It can be shown that

$$C \sim \frac{2 \epsilon_0 dL}{3 d_{CNT}}$$

When the two CNTs touch each other,

we have $\delta = d_{cnt}/2$.

Next we note that the electrostatic ($F_{electrostatic} = -\frac{\partial E_{electrostatic}}{\partial x}$) and van der Waals

$$(F_{vdW} = -\frac{\partial E_{vdW}}{\partial x}) \text{ forces are both attractive while}$$

the elastic force ($F_{elastic} = -\frac{\partial E_{elastic}}{\partial x}$) is not. Thus, at

$$-\frac{\partial E_{total}}{\partial x} = 0, \text{ the total forces acting on the CNTs}$$

cancel out and result in a stable configuration. When $F_{vdW} \geq F_{elastic}$ ($V=0$ V) the van der Waals forces overcome the elastic force and CNTs can latch onto each other. Clearly this situation should be achieved after application of a voltage pulse because otherwise, the CNTs' will spontaneously clamp onto each other. This simple but important observation puts a limit on how close CNTs can be to each other.

The above equations can be solved to study scaling laws of CNEMS and design devices with different feature sizes and characteristics. To demonstrate feasibility of switching and latching with reasonable voltages and device structures, we consider the CNEMS structure schematically shown in Fig. 1. Taking $d_{cnt} \sim 20$ nm, and $L=50$ nm, and $d_1 \sim 3$ nm, $d_2 \sim 3.5$ nm, we calculate $E_{elastic} \sim 34$ eV while $E_{vdW} \sim 740$ eV. The two energies are equal at $L \sim 19$ nm for $d \sim 3.5$ nm and d_{cnt} of 20nm ($\delta \sim 10$ nm). The electro-static potential needed to bend the 50nm-long CNT to achieve deflection of $\delta \sim 10$ nm is around 10 V (this is calculated by setting $E_{electrostatic} \sim E_{elastic}$). In subsequent switching, however, this voltage will be dropped to around 1 V since a large portion of the elastic energy stored in the CNT will be recovered.

Based on the above considerations, we note that $V_{th} \sim 10$ V dropping to ~ 1 V after the initial cycle as shown in Fig. 2. The main reason for this reduction is that the stored elastic energy causes the center CNT (CNT1 in Fig. 1) to spring back towards the CNT3 when it is released from CNT2. The van der Waals force latching CNT1 and CNT2 is almost entirely balanced out as soon as CNT1 and CNT2 are charged with the same polarity.

To calculate the switching speed, we note that the resonant frequency of a CNT (see Fig. 1) is given by:

$$\omega = \sqrt{\frac{8EI}{mL^3}}, \text{ where "m" is the CNT's mass and the}$$

rest of parameters are defined above. For $L \sim 50$ nm, the radial frequency is around 3.16×10^{11} radian/s corresponding to a frequency of 50 GHz. This yields a transition speed ($v_t \sim \omega L$) of around 1.6×10^4 m/s that results in transition time ($\tau \sim \delta/v_t$) of around $10^{-12} - 10^{-10}$ s. The charging time constants may limit the CNEMS speed in the final circuits.

The device isolation resistance in "off" state can be calculated using the tunneling current between two adjacent and non-contacting CNTs as $I \sim I_0 e^{-d_{cnt}/\lambda}$ where λ is approximately the De Broglie wavelength (~ 10 Å) and $I_0 \sim 0.1$ μ A (@ 1V). For $d_{cnt} \sim 20$ nm, I is

approximately 2×10^{-16} A that yields an isolation resistance of around 5×10^{15} Ω .

The device resistance in the "on" state is given by the sum of contact resistances, the two CNT resistances and the CNT-CNT contact resistance. With good titanium carbide or Pd contacts to the CNTs, the contact resistance can be made small (~ 1 k Ω). The CNT-CNT contact resistance when the two CNTs are touching with an overlap of 30-50nm, is also very small (this will be dictated by tunneling in clean CNTs). The overall resistance will be around 10 k Ω (for $\rho_{cnt} \sim 1$ k Ω -cm).

CNEMS's operation depends on CNT diameter, length, location, and conductivity. We have developed a metal-catalyzed chemical vapor deposition growth technique that results in the growth of multi-walled and single-walled carbon nanotubes that are self-aligned and self-welded to silicon posts as shown in Fig. 3. The CNT diameter depends on the diameter of the catalyst particles, growth temperature and gas flow rates. These parameters are readily controlled to yield uniform CNT diameter.

i) Programming CNEMS

The CNTs will be programmed by applying voltage pulses to attract and latch adjacent CNTs to allow for setting the current path in the circuit.

ii) Re-setting and Isolating CNEMS

To "un-stuck" all the CNTs in the device, we will integrate an electrode under the CNTs so that when a voltage is applied between the bottom electrode and the CNTs, the CNTs are attracted to the bottom electrode that will be covered with a thin oxide layer to prevent current flow but to enable electrostatic actuation. The distance between the CNTs and bottom electrode will be set around 25nm so that the elastic energy of the bent CNTs will be larger than the van der Waals force to prevent latching with the bottom surface. Thus, after the resetting pulse is applied, the CNTs will return to their initial pre-programmed state.

iii) Scaling Laws

Clearly CNTs can be scaled down to 1nm diameter and sub-10nm lengths. The main constraints are how large of an initial programming threshold voltages are allowed and how precisely CNT-CNT distances can be controlled in the fabrication process. The main issues dictating scalability are threshold voltages and placement precision.

3. Circuit Implementation

As described in Section 2, the proposed CNEMS has fundamentally different principle of operation compared to conventional MOSFET switch. Thus, developing logic circuits and memory array out of

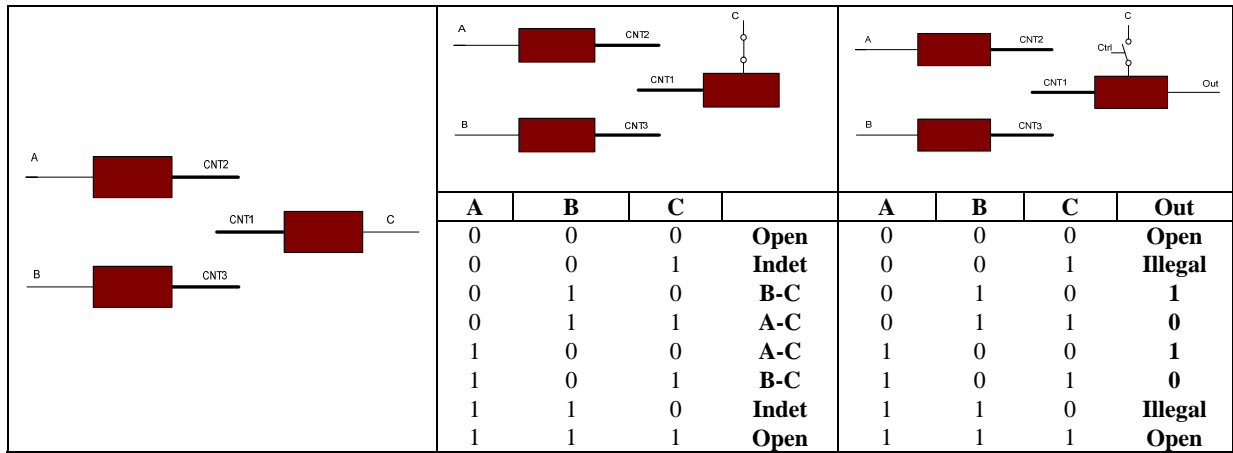


Figure 4. a) Schematic of the CNEMS.

b) Programming CNEMS.

c) Logical behavior of CNEMS.

these new devices require a major shift in design methodology.

3.1. Basic Logic Functions

To understand how the proposed switch can be used to realize logic function, let us discuss behavior of the switch in terms of logical operation. Fig. 4(a) depicts the schematic diagram of the switch, which has three terminals A, B and C.

Depending on the voltage differential between the terminals, either A or B (not both) may be connected to terminal C. For a given voltage at A and B, we can consider C as the controlling terminal (analogous to the GATE terminal in a MOSFET switch), which determines configuration of the switch. However, unlike MOSFET switch or conventional MEMS (Micro Electro-Mechanical Switch), the complementary nature of the CNEMS does not allow a signal path between B and C, which dictates that the logic styles using MOSFET cannot be readily used in realizing logic function with CNEMS switch. From Fig. 4(b), we can observe that by using two-valued logic, CNEMS switch can be taken to one of the four states. Apart from the two states discussed earlier (where terminal C is connected to either A or B), the

switch may be completely open (C is not connected to any of A or B) when all terminals have the same voltage or state of the switch may be indeterminate, when both A and B have the same voltage difference with respect to C. In the later case, position of the switch will eventually depend on the relative strength of the CNTs at A and B, which will be determined by design marginalities like process variations. This state therefore, should be considered as “illegal” with respect to logic design. It can be observed that the switch can be used for pass-transistor like logic implementation. However, it requires two steps to evaluate the logic. In the first step, terminal C can be used to configure the switch by applying appropriate voltage differential. In the second step, terminal C should be disconnected from the controlling input and treated as the output. Fig. 4(c) shows the truth table for the logic operation of the switch with C as controlling input. It can be noted that output terminal has a valid state as long as $A \oplus B = 1$.

Implementation of logic gates similar to pass transistor or static CMOS logic the CNEMS device requires special consideration to avoid illegal or unstable states. However, logic functions can be realized efficiently using small memory array

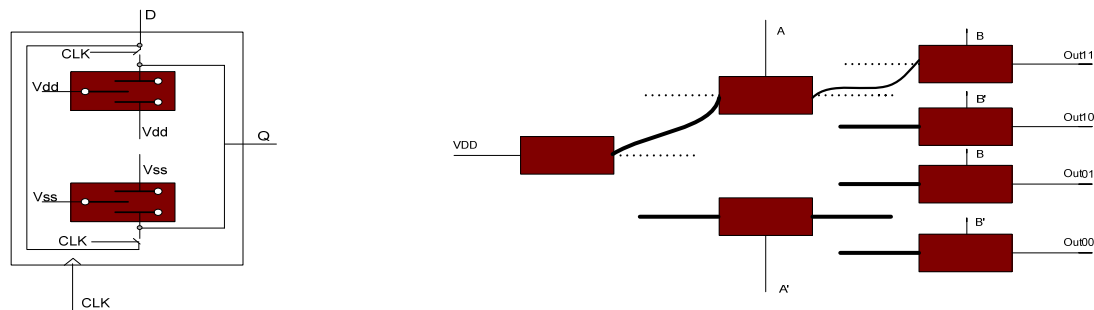


Figure 5. a) An inverting flip-flop using the CNEMS device.

b) Configuration of a decoder (2X4) for A=1, B=1, implemented with CNEMS

organized as look-up table (LUT), as used in conventional SRAM-based FPGA [16]. Schematic of an inverting flip-flop is shown in Fig. 5(a) using two CNEMS switch configured similar to a conventional static CMOS inverter. The flip-flop can be used to realize the sequential elements in a system. The CNEMS can also be used, in interesting ways, to realize complex functions with minimum number of switches. For example, Fig. 5(b) describes a customized implementation of a decoder circuit (2X4), which requires considerably less number of primitive switches than possible using conventional logic synthesis approach. Note that once the CNTs latch properly creating a signal propagation path on application of voltage pulse in the CNEMS terminals, input signals (A, A', B, and B') are disconnected (using isolation switch) during evaluation phase.

The proposed logic implementations have robust switching operation, low active power for switching states (along with very small leakage), as well as high switching speed (since the transport between connected terminals are ballistic, switching speed is determined by the transition speed of the CNTs).

3.2 Memory

One of the interesting features of the proposed device is that each switch can be easily configured as a non-volatile memory element. Unlike the charge-based memory design using MOSFET switch (both static and dynamic RAM), these memory elements can have high data retention capability due to very low leakage current. Fig. 6 depicts the schematic of a CNEMS-based memory array, which has an organization similar to conventional 6-T static RAM [10]. Note that here, each cell is an inverting data storage element, which can be programmed to connect to either VDD or GND based on the voltage applied on terminal 1. The data input is connected to terminal 1 of the switch via an isolation switch, which connects the data input during the write operation (determined by the "Wr" signal) and disconnects after the write operation is completed. Once the write data is disconnected, the bottom terminal (terminal 3) voltage is changed to VDD and the cell retains its content until the next write cycle reprograms the cell. Bitline (BL) works as data input signal during write operation, while the word lines (WL_i) select a particular memory codeword for read or write operation. During the read operation, the bottom terminal voltage is changed to GND and a voltage of VDD/2 is applied on the bitline. Since the memory cell stores an inverted value, the data retrieved from each cell needs to be inverted after reading to restore the original data. As observed from Fig. 6, each memory cell consists of just three CNEMS switches (two of which are configured as isolation device) and thus can

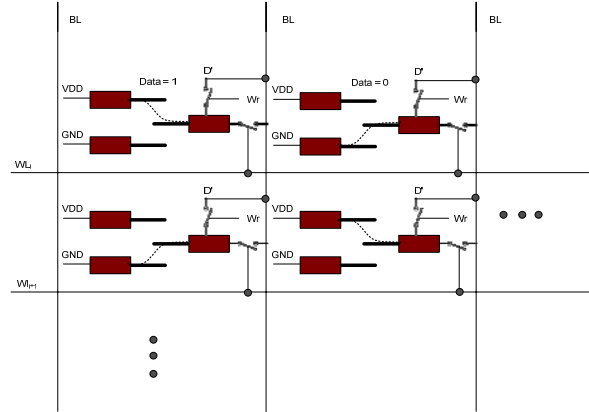


Figure 6. Design of memory array using CNEMS

help to achieve very high integration density. Note that besides achieving high integration, the memory implementation using CNEMS alleviates two major design concerns with modern memory system. 1) It greatly reduces stand-by leakage from the memory cache allowing low-power embedded memory design and 2) due to its high data retention capability, it has potential to replace the off-chip dynamic memory (DRAM), which requires periodic refreshing to avoid retention failures [10].

It is worth noting that the read/write operations in the CNEMS based memory can be accomplished with low active power. Once the memory cell is programmed, the read operation does not induce any transition in the core CNEMS (that stores the value). Hence, the only active energy dissipated during read operation is in switching the two isolation devices per cell. During write operation the core cells can make a transition (depending on the data to be written). However, the transition energy in the cell can be considerably reduced after the initial programming of the cells due to the elastic energy stored in the CNTs. The proposed memory cell can also be used to design high-performance register files, where the data storage elements are typically designed with dynamic logic circuits for high access speed [13]. It is worth noting that since memory cell implemented with CNEMS device is not charge-based, the stored value does not flip due to alpha or neutron particle hit [17], and hence, completely immune to soft error.

4. System Architecture

With the logic and memory implementation strategies described in Section 3, one can proceed with a system design. Although the conventional architectural paradigms used in traditional CMOS based system design can be used for CNEMS, the unique properties of these devices can be exploited to innovate novel and efficient architectures. Since these devices can be configured as a non-volatile memory

element (Section 3), it can be used to develop look-up table based reconfigurable architecture (like Xilinx virtex family [16]), which allows high-speed dynamic reconfigurability. The architecture can be efficiently updated during field operation and due to the non-volatile nature of the memory elements, system configuration will not be lost at power off, i.e. the system will be “instant on”.

Since CNEMS device has order of magnitude less “ON” resistance compared to a CMOS device of the equivalent physical parameters, CNEMS can be used to develop high-speed programmable interconnect used in many reconfigurable architecture. Moreover, unlike the traditional programmable interconnect, where the switch configuration is loaded in SRAM cells, we do not need SRAM cells for CNEMS device. Therefore, switch modules in reconfigurable architecture can be developed using CNEMS with significantly higher integration density and lower power.

System implementation with these devices, however, requires consideration of the impact of manufacturing defects, process imperfections as well as transient defects. As mentioned in section 2, CNEMS devices can suffer from variations in CNT diameter, length, bias voltage etc. along with a number of defect mechanisms that result in non-operational CNEMS switch. Although a complete investigation of defect mechanism and behavior of the device under defect or process variation is not performed yet, we can provide architecture-level fault-tolerance to achieve reasonable manufacturing yield and to ensure robustness of operation. We propose a reconfigurable architectural framework where on-chip hardware resources can be reconfigured for defect tolerance and performance optimization.

Fig. 7 describes the overall architecture of a system, which has dedicated datapath, controller, buses and embedded memory along with a flexible hardware, which can be configured on demand to either a memory array or a set of datapath elements or any combination of them. Note that to avoid the overhead of a fully reconfigurable system, we consider reconfiguration into only a part of the entire hardware resources, while other parts are dedicated to specific logic or memory implementation. The flexible resource can be reconfigured to either replace a failing datapath or register location, or dynamically transform into a special datapath (such as the ones used in streaming

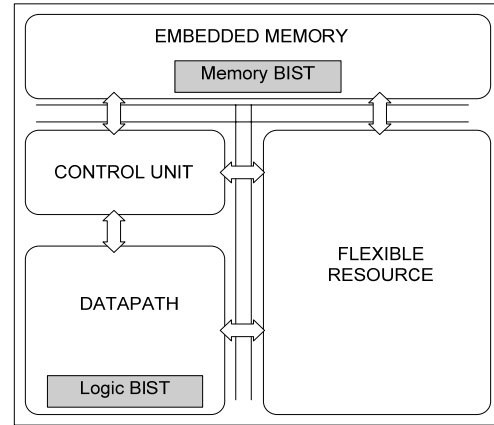


Figure 7. Overall architecture of a reconfigurable system using CNEMS. The flexible resource can be configured to implement either datapath element or memory.

applications e.g. image encoder/decoder) or memory array (for data intensive applications) depending on the particular application it is running. Datapath and memory modules will have their respective Built-In Self Test (BIST) unit to identify manufacturing defects, process imperfections, and transient defects.

Fig. 8(a) describes the organization of the flexible resource. Similar to conventional SRAM-based FPGA implementations [15], the proposed organization of the flexible resource comprises of a two-dimensional array of alternating configurable logic/memory block and programmable switch module. Inside a switch block, connections for wires of length 1 are implemented using six switches as described in Fig. 8(b). These switches can be configured by applying the control signals at three terminals of the switch. However, once these switches are configured, it does not require storing the configuration bit in a SRAM cell. As mentioned earlier, the “ON” resistance of CNEMS switches is considerably lower than the “ON” resistance of CMOS transistors for equal width. Thus,

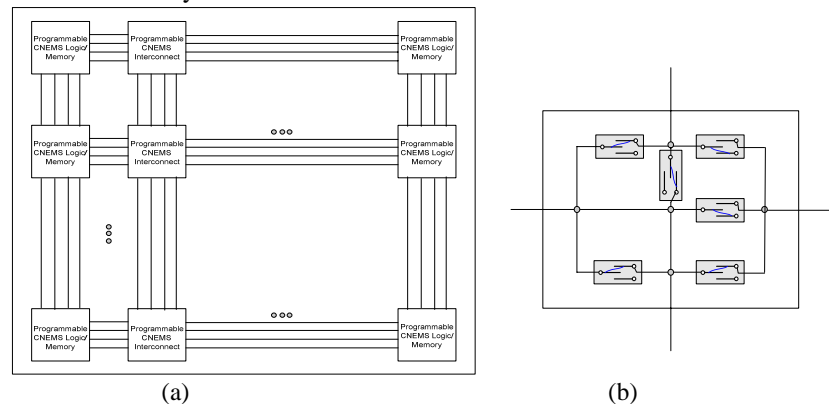


Figure 8. a) The organization of the flexible resource as a two-dimensional array of programmable logic/memory blocks and programmable switches; b) implementation of a bidirectional programmable interconnect using CNEMS.

the proposed switch module can be very efficient in reducing propagation delay for long interconnect. Moreover, the absence of SRAM configuration switches reduces power dissipation and die area.

Fig. 9 shows the block diagram of the programmable logic/memory block. It consists of two look-up tables, each with four storage bits that can implement any two-input Boolean function. The programmable logic/memory block can be extended to implement three or four input functions by incorporating larger LUTs. One important difference between the proposed programmable block and conventional configurable logic block (CLB) [15, 16], is that the proposed block does not require additional flip-flop for storing data. Instead, the LUTs in the proposed programmable block can be configured to realize four flip-flops. Thus it can be configured in two possible modes: a) to implement two Boolean functions or b) to implement four storage elements. Note that, if we have 32 programmable logic blocks in a row of the flexible resource (Fig. 8(a)), by configuring all of them in mode (b), we can realize four 32-bit registers (first bit of all blocks constitute the first register), which can be addressed by one of the two decoders inside the programmable blocks. As can be seen in Fig. 5(a) and Fig. 9, elements in the LUTs can be easily reconfigured to implement a register bit.

5. Conclusion

We have proposed a novel Nano Electro-Mechanical switch that exploits unique properties of carbon nanotube. We have successfully manufactured the device and evaluated its switching properties. Two most important features of this device are its internal energy storage for ultralow-power operation and its easy configurability into a non-volatile memory element. The device is amenable to memory array design with high integration density and look-up table based logic implementation. Finally, the device can be used to develop a reconfigurable fabric, which allows high-speed dynamic reconfigurability of the CNEMS switches into either logic function or memory. Unlike conventional FPGAs the LUTs can be easily configured into register bank for data storage.

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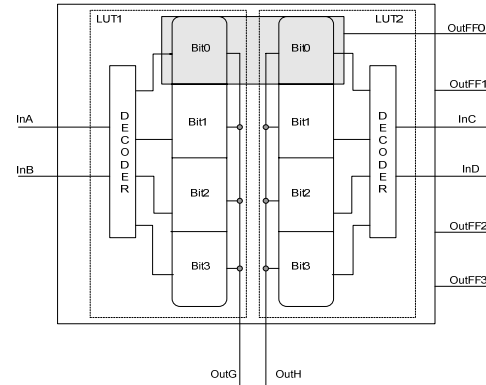


Figure 9. Implementation of the programmable logic/memory block using look-up tables.

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