FABRICATION AND TESTING OF SINGLE CRYSTALLINE 3C-SIC DEVICES USING A NOVEL SIC-ON-INSULATOR SUBSTRATE

Hung-I Kuo, Christian A. Zorman, and Mehran Mehregany
Department of Electrical Engineering and Computer Science
Case Western Reserve University, Cleveland, Ohio 44106

ABSTRACT

Single crystal, 3C-SiC lateral resonant structures and piezoresistive strain gauges were fabricated on a novel SiC-on-Insulator (SiCOI) substrate. The SiCOI substrates were fabricated using a bonding-free, substrate growth and etch-back method that bypasses the problems associated with conventional methods to produce dielectrically-isolated 3C-SiC films. The process works equally well with SiO_2 and stoichiometric Si_3N_4 layers since bonding is not used; additionally, surface micromachining is enabled when SiO_2 is used. Lateral resonators fabricated from the 3C-SiC films exhibited Q values as high as 103,000. Using the 3C-SiC strain gauges, the π_{11} piezoresistance coefficient was the largest, with a value of -17.8×10^{-11} Pa^{-1}.

INTRODUCTION

3C-SiC is a leading material for harsh environment and high-frequency MEMS applications due to its outstanding electrical, chemical and mechanical properties in conjunction with its compatibility with Si processing techniques. Recently, attention has shifted to polycrystalline 3C-SiC since it can readily be deposited on dielectric layers such as SiO_2 and Si_3N_4. Some device components, such as piezoresistors, however, perform better if single crystal material is used, and in the case of 3C-SiC, work best when they are electrically isolated using insulating substrate layers. SiC-on-Insulator (SiCOI) wafers offer this possibility. When SiO_2 is used as the insulating layer, these substrates become attractive for single crystal SiC surface micromachined devices since the buried oxide layer can be used as a sacrificial layer while providing electrical isolation of micromachined structures.

The most commonly used method to produce 3C-SiC SiCOI substrates is direct epitaxial growth of 3C-SiC films on various commercially-available SOI wafers. This method works well in producing large-area substrates, but a Si layer sandwiched between the 3C-SiC and SiO_2 layers is often created. Fusion bonding has also been used to fabricate these substrates, but unfortunately bonding yields are often low due to excessive warpage of the 3C-SiC coated wafers and high surface roughness of the 3C-SiC films.

This paper reports on the fabrication of dielectrically isolated 3C-SiC surface micromachined lateral resonators and piezoresistive strain gauges for bulk micromachined pressure sensors using a novel, bonding-free method to fabricate large area 3C-SiC-on-insulator wafers [1]. The process bypasses the problems associated with wafer bonding altogether by using a high deposition rate polysilicon process in conjunction with wet chemical etching to produce wafer-thick polysilicon layers that serve as substrates for the 3C-SiC-on-insulator (SiCOI) structures [1]. These substrates offer unique opportunities to fabricate structures from single-crystal 3C-SiC that would otherwise be very difficult using alternative approaches.

SUBSTRATE FABRICATION

A schematic of the key steps in the fabrication process of a 3C-SiC on SiO_2 substrate is shown in Fig. 1. The process begins with the acquisition of 100-mm diameter, 700 micron-thick silicon (100) wafers. A 3C-SiC film is heteroepitaxially grown on each wafer in a rf-induction-heated, cold wall reactor sized to grow films on two 100 mm-diameter Si wafers. 3C-SiC films are grown using a conventional, carbonization based two step APCVD process detailed elsewhere [2]. The process uses C_3H_8 and SiH_4 as source gases and H_2 as a carrier gas. The growth temperature is 1280°C.

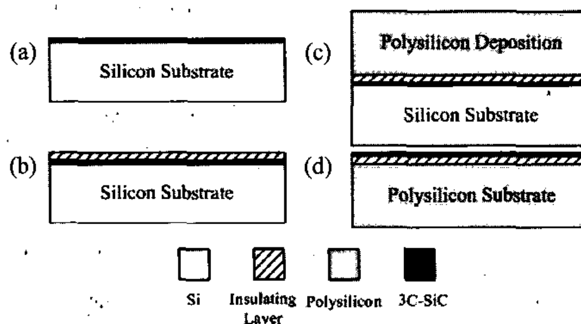


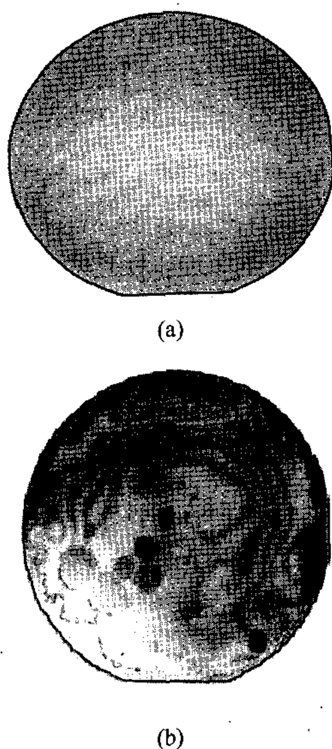
Figure 1. Cross-sectional schematics of the 3C-SiC-on-SiO_2 substrate fabrication process **(a)** after 3C-SiC growth, **(b)** after polysilicon oxidation, **(c)** after thick polysilicon deposition, and **(d)** after Si removal.

Following film growth, the surface of the 3C-SiC film is mechanically polished to reduce surface roughness. After polishing, the insulating layer is prepared. A SiO_2 layer is prepared by completely thermally oxidizing a LPCVD polysilicon thin film. In this manner, a thermal oxide thickness in excess of 1.5 μm is grown in a reasonable amount of time on the 3C-SiC surface, a process not feasible from a time and material point of view if direct thermal oxidation of 3C-SiC were used. When desired, a stoichiometric Si_3N_4 layer deposited by LPCVD can be used in place of SiO_2. After adding the insulator layer, thick (~600 μm) polysilicon is deposited on it. The polysilicon is deposited using a silane-based epi-like process designed for high deposition rates. The net effect of the deposition process is a wafer-thick polysilicon layer that is nearly stress balanced with the single crystal wafer, in part because

0-7803-7731-1/03/$17.00 ©2003 IEEE

the thermal mismatch is negligible, but also because the thickness of each silicon layer is roughly equivalent. The process essentially sandwiches the 3C-SiC and insulating thin film between two very thick Si layers. After this step, the wafer is ready for the 3C-SiC transfer etch. First, a protective SiO_2 layer is grown on the backside of the polysilicon substrate. The entire sample is then immersed in KOH, which etches the unmasked (100) Si wafer and stops on the 3C-SiC film, resulting in the creation of a 3C-SiCOI substrate. If needed, additional 3C-SiC is grown on the 3C-SiC surface by a homoepitaxial process [3].

Because bonding is not employed, insulators of various materials (SiO_2 and Si_3N_4) and thicknesses can be easily utilized. Moreover, the orientation of the 3C-SiC film is determined by the Si substrate used during 3C-SiC epitaxy, therefore SiCOI wafers incorporating (100), (111) and (110) 3C-SiC films can be fabricated. Using this method, transfer rates over 99% are readily achievable, as compared with only 60% using wafer bonding. Figure 2 compares 3C-SiC on Insulator substrates made by the substrate growth and wafer bonding methods.



(a)

(b)

Figure 2 100 mm-diameter, 3C-SiC-on-Insulator wafers prepared by (a) thick polysilicon growth, and (b) wafer bonding. Note the delaminated regions on the wafer in (b).

DEVICE FABRICATION AND TESTING

1. Piezoresistive 3C-SiC Strain Gauges

The 3C-SiC on insulator wafers offer an effective and convenient means to evaluate the piezoresistive properties of single-crystal 3C-SiC films since dielectrically-isolated, piezoresistive strain gauges can be fabricated directly from these substrates. As such, 3C-SiC strain gauges of several configurations were fabricated on 30 mm x 5 mm cantilever beams cut from the SiCOI wafers. An example of one such configuration is shown schematically in Fig. 3. The 3C-SiC films were 2 μm thick and had a nominal resistivity of 0.18 Ω-cm. The films were not intentionally doped, but nonetheless exhibited n-type conductivity due to unintentional nitrogen doping from residual N_2 in the reaction chamber and C_3H_8 source gas. The piezoresistors were patterned by RIE using a $CHF_3/O_2/He$ plasma detailed elsewhere [4]. A 4000 Å-thick aluminum film was deposited by sputtering and patterned to form conducting lines from the inner measurement locations to outer contact pads.

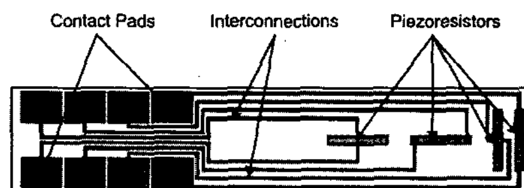


Figure 3. Schematic diagram showing the arrangement of 3C-SiC piezoresistors on a cantilever beam diced from a SiCOI wafer.

The strain gauges were tested using the custom-built cantilever displacement apparatus showed in Fig. 4. The apparatus could be used to displace the cantilevers distances up to 500 μm. Cantilevers were clamped to a vise that held the specimen in a horizontal position. Wires fitted with custom, miniature clips were used to make electrical connections between the strain gauge contact pads and a precision ohmmeter. A custom-made screw dial meter was positioned under the tip of each beam and was used to provide the mechanical displacement. A digital micrometer was used to measure the tip displacement of the cantilever.

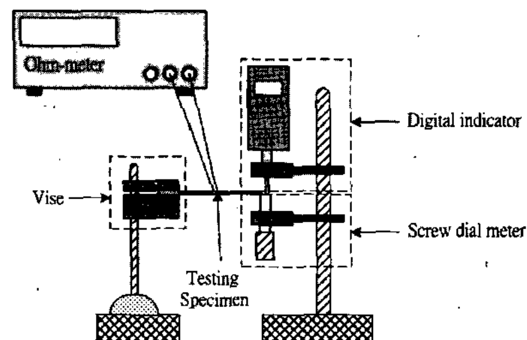


Figure 4. Schematic of the experimental measurement set-up for the 3C-SiC piezoresistive strain gauges.

Table 1 presents a summary of the piezoresistance coefficients measured for the 3C-SiC films investigated in this study, as well as another study in which the piezoresistance coefficients for 3C-SiC were measured

using a similar technique [5]. It is clear from Table 1 that the values for p_{11}, p_{12}, and p_{44} reported here are smaller than those reported in [5]. We speculate that this difference arises from the fact that the 3C-SiC samples measured in [5] were much thicker (10 μm) and the resistivity was higher (0.7 Ω-cm) than in this work (2 μm and 0.18 Ω-cm). It is well known that the defect density in 3C-SiC films grown on Si is quite high at the film/substrate interface, but decreases substantially with increasing thickness. It is not surprising, therefore, that thin 3C-SiC films would have lower piezoresistance coefficients since piezoresistivity is dependent on crystal quality. It should also be noted that the measurements in [5] were over a wider range of strain (0–1800 ppm) than this work (0–70 ppm). The approach presented here focuses on a smaller range of the strain, which is more representative of operational range for micromachined pressure sensors. The largest measured piezoresistive coefficient for the n-type films in this study was π_{11} at -17.8×10^{-11} Pa^{-1}. P-type 3C-SiC films were not studied, but the fabrication methods used here do not preclude this possibility.

	Thickness (μm)	Resistivity (Ω-cm)	π_{11} ($10^{-11}Pa^{-1}$)	π_{12}	π_{44}
3C-SiC	2	0.18	-17.8	10.0	4.4
3C-SiC [2]	10	0.7	-31.8	19.2	5.2

Table 1. A comparison of the piezoresistance coefficients of 3C-SiC films measured using the cantilever beam method.

2. 3C-SiC Lateral Resonant Devices

The SiCOI substrates detailed in this paper offer unique opportunities to fabricate single crystal, 3C-SiC structures of different crystal orientations using surface micromachining techniques. For this study, we elected to fabricate lateral resonant structures, since such devices can be fabricated from a single structural layer and are relatively easy to test electrically. The designs used in this study were electrostatically actuated comb drive resonators with relatively large shuttles, long suspension beams and numerous interdigitated comb fingers.

Fabrication of the lateral resonators was restricted to the SiCOI wafers having SiO_2 as the insulating layer, since this layer could be used both for sacrificial release and electrical isolation. The SiC patterning process was the same as used for the piezoresistive strain gauges as described previously. After patterning by RIE, the wafers were diced, and the aluminum mask was removed. The devices were then released by a timed etch of the sacrificial oxide in HF for approximately 5 minutes. Figure 5 shows a SEM picture of a typical 3C-SiC lateral resonator used in this study along with a close up of the interdigitated comb fingers. SiCOI wafers with 2 μm-thick, (100), (110), and (111) 3C-SiC films were used in the fabrication process. Due to issues related to high residual stresses, the (111) 3C-SiC devices did not survive the release step.

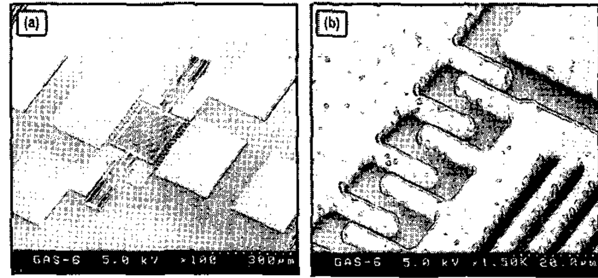


Figure 5. SEM micrographs of **(a)** a (100) 3C-SiC lateral resonator of the type used in this study, and **(b)** a close up SEM image of the lateral resonator detailing the interdigitated comb fingers.

The lateral resonators were packaged onto printed circuit boards that enabled testing using a two-port configuration. A schematic is shown in Fig. 6. In this configuration, a DC voltage, V_P, was used to bias the shuttle. An AC signal, v_i, generated by an Agilent 4395A network analyzer, was applied onto one of the ports. The shuttle resonated when the AC signal reached its mechanical resonant frequency. This resulted in a motional current at the other port [6], which was amplified by a Philips SA5211 transimpedance amplifier that in turn transferred the motional current into an output voltage output. The output voltage was analyzed using a network analyzer. Resonator testing was conducted in a custom-built vacuum chamber that could reach pressures as low as 15 μTorr for testing.

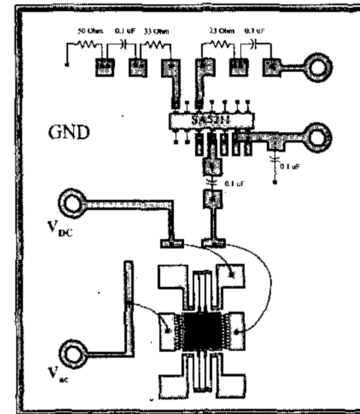


Figure 6. Schematic diagram of the PCB used for electrical testing of the lateral resonant devices.

Testing of the (100) and (110) 3C-SiC resonators was performed at pressures ranging from 760 Torr to 15 μTorr in order to characterize the effect of pressure and crystal orientation on the quality factor (Q) of the devices. Figures 7 and 8 show typical transmission spectra for a (100) 3C-SiC resonator tested at 1 Torr and 15 μTorr, respectively. In both cases, Q could be extracted from the spectra. It should be noted that the spectra collected from the (110) 3C-SiC devices were virtually indistinguishable in appearance from those shown in Figs. 7 and 8 and thus are not presented here.

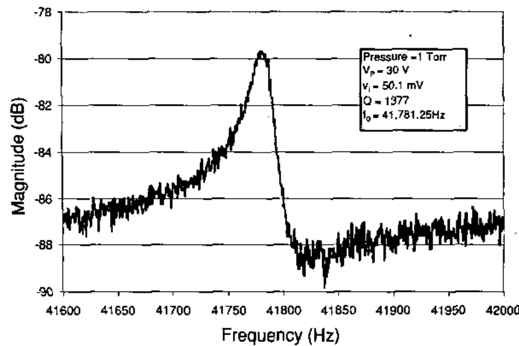


Figure 7. Transmission spectrum for a (100) 3C-SiC lateral resonator measured at 1 Torr.

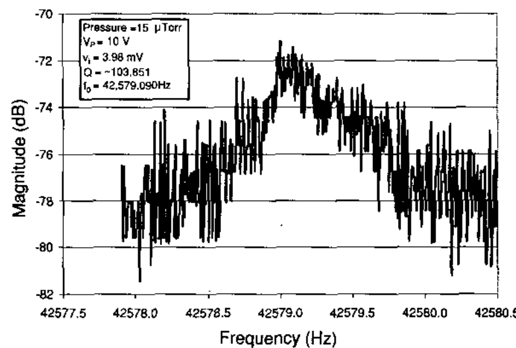


Figure 8. Transmission spectrum for a (100) 3C-SiC lateral resonator measured at 15 µTorr.

The highest achievable Q for (100) 3C-SiC lateral resonators was about 103,000 at 15 µTorr, whereas the highest Q for the (110) oriented devices was about 77,000, also at 15 µTorr. Figure 9 compares the quality factors of (100) and (110) 3C-SiC lateral resonator tested at various pressures. (100) 3C-SiC resonators exhibited a higher Q than (110) 3C-SiC resonators at all pressures, perhaps due to a higher level of crystal quality in the (100) 3C-SiC films.

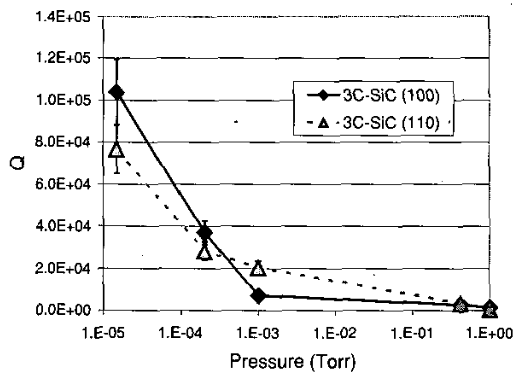


Figure 9. A comparison of the quality factor (Q) versus pressure for (100) and (110) 3C-SiC lateral resonators.

From the resonant frequency data, the Young's modulus for (100) 3C-SiC was determined to be 359.5 ± 45 GPa. This finding is quite consistent with results reported from similar films measured using the bulge test [7]. The difference in the average resonant frequency between the (100) and (110) 3C-SiC resonators was only about 0.2%, which is within the error of the measurement. This suggests that (100) and (110) 3C-SiC could have the nearly the same Young's modulus. To the best of our knowledge, this study is the first to measure the Young's modulus for epitaxially grown (110) 3C-SiC, therefore no comparison with other results could be made.

ACKNOWLEDGEMENTS

The authors thank R. Jezeski for operating the SiC reactor. This work as supported by DARPA/MTO (Grant # DABT63-98-1-0010).

REFERENCES

[1] H. Kuo, "Fabrication and Applications of 3C-Silicon Carbide Wafers by Grow-A-Substrate Method on Insulator", Ph.D. Dissertation, Case Western Reserve University, August 2002.

[2] C.A. Zorman, A.J. Fleischman, A.S. Dewa, M. Mehregany, C. Jacob, S. Nishino, and P. Pirouz, "Epitaxial Growth of 3C-SiC Films on 4 in. diam (100) Silicon Wafers by Atmospherics Pressure Chemical Vapor Deposition", *J. Appl. Phys.* **78**, 5136-5139, (1995).

[3] K.N. Vinod, C.A. Zorman, A. Yasseen, and M. Mehregany, "Fabrication of Low Defect Density 3C-SiC on SiO_2 Structures Using Wafer Bonding Techniques", *J. Electron. Mat.*, **27**, L17-L20, (1998).

[4] A.J. Fleischman, C.A. Zorman, and M. Mehregany, "Etching of 3C-SiC Using CHF_3/O_2 and $CHF_3/O_2/He$ Plasmas at 1.75 Torr", *J. Vac. Sci. and Tech. B*, **16**, 536-538, (1998).

[5] J. Shor, D. Goldstein, and A. Kurtz, "Evaluation of β-SiC for Sensors", *Proc. Transducers 91*, 912-915, (1991).

[6] C. Nguyen, "Micromechanical Signal Processors", Ph.D. Dissertation, Univ. of California at Berkeley, (1994).

[7] J. Mitchell, "Characterization of Mechanical Properties of Cubic Silicon Carbide Thin Films Deposited Onto Silicon", MS Thesis, Case Western Reserve University, January 2001.