Oversampled Capacitance-to-Voltage Converter IC with Application to SiC MEMS Resonator

S. Lei, S. Garverick, S. Stefanescu, C. Zorman
Dept. of EECS
Case Western Reserve University
Cleveland, OH 44106, USA

ABSTRACT

This paper reports the first electronic circuit used to measure MEMS resonator motion in the time domain. The measurement of shuttle position is made using a capacitance-to-voltage converter IC that has been developed by combining correlated double sampling with delta modulation in a fully differential circuit topology. This oversampling circuit may be adjusted to trade bandwidth (sample rate) for resolution, while reference level may be adjusted to set the desired sensitivity to accommodate a large range of capacitive sensor interface applications. For example, test results demonstrate a resolution of 170 aF for a signal bandwidth of 3 kHz, a 68-dB dynamic range, and nonlinearity less than 0.16%.

1. INTRODUCTION

MEMS sensors for acceleration, pressure, and shear stress typically produce signals that require capacitance sensing with sub-fF resolution and sample rates up to 1 ksps. MEMS lateral resonators can be used as the basis of stable oscillators and/or sensors, and have resonant frequencies on the order of 20 kHz with capacitance < 10 fF. The time varying capacitance of such resonators must be sampled at rates near 1 Msps.

The performance of microfabricated capacitive sensors is often limited by interference and noise that is exacerbated by parasitic packaging capacitance that is many orders of magnitude greater than the sensor capacitance. Monolithic fabrication of a sensor with its interface electronics is desirable since the parasitic capacitance on the sensing node can be better shielded from interference. However, a fully integrated process is technically challenging and expensive. For this reason, approaches that combine partial on-chip and partial off-chip electronics have been explored.

Bramani proposed a method to measure capacitance variation by measuring the phase shift between voltage and current in a series RLC circuit tuned to resonance [1]. In [2, 3], Toth, et al and Goes, et al proposed a method to measure capacitance by forming an oscillator using the sensor capacitor. In [4], off-the-shelf components were used by Mochizuki, et al, to make an interface circuit to measure capacitance ratio. Kung, et al [5] presented a charge redistribution technique for capacitor sensing. Switched-capacitor techniques are very suitable for this application, in general [6].

In this paper, a flexible capacitance-to-voltage (C-to-V) converter IC is reported that achieves the performance required for demanding MEMS applications, despite packaging capacitance much larger than the sense capacitance. The IC uses correlated double sampling (CDS) in combination with delta modulation, as first reported by Ranganathan, et al [7]. The CDS technique acts as a high-pass filter that eliminates low-frequency noise and interference, while the oversampling provides averaging of the high-frequency noise.

2. SYSTEM ARCHITECHTURE

A simplified block diagram of our capacitance-to-voltage converter IC is shown in Fig. 1. The sensor capacitance is first converted to a discrete-time voltage signal using a switched-capacitor amplifier. The double-sampler removes offset and low-frequency noise from the voltage signal. Finally, a delta modulator provides averaging and produces a continuous-time voltage output in proportion to the signal, as well as a binary bit-stream in proportion to the derivative of the capacitance signal.

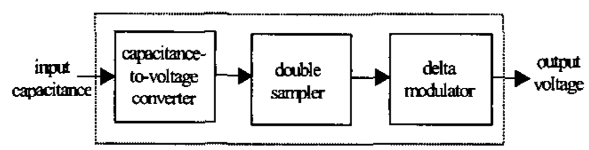

Figure 1: Block diagram of the capacitance-to-voltage IC.

A simplified circuit schematic of the IC is presented in Fig. 2. The sensor signal is represented by the difference between C1 and C2. A single-ended sensor can be accommodated using a fixed reference capacitor that is adjusted to the center of the sensor range.

All the major building blocks are implemented with fully differential topologies for better immunity to interference, and most circuits in the signal path use switched-capacitor techniques. The IC simply accepts a master clock at a

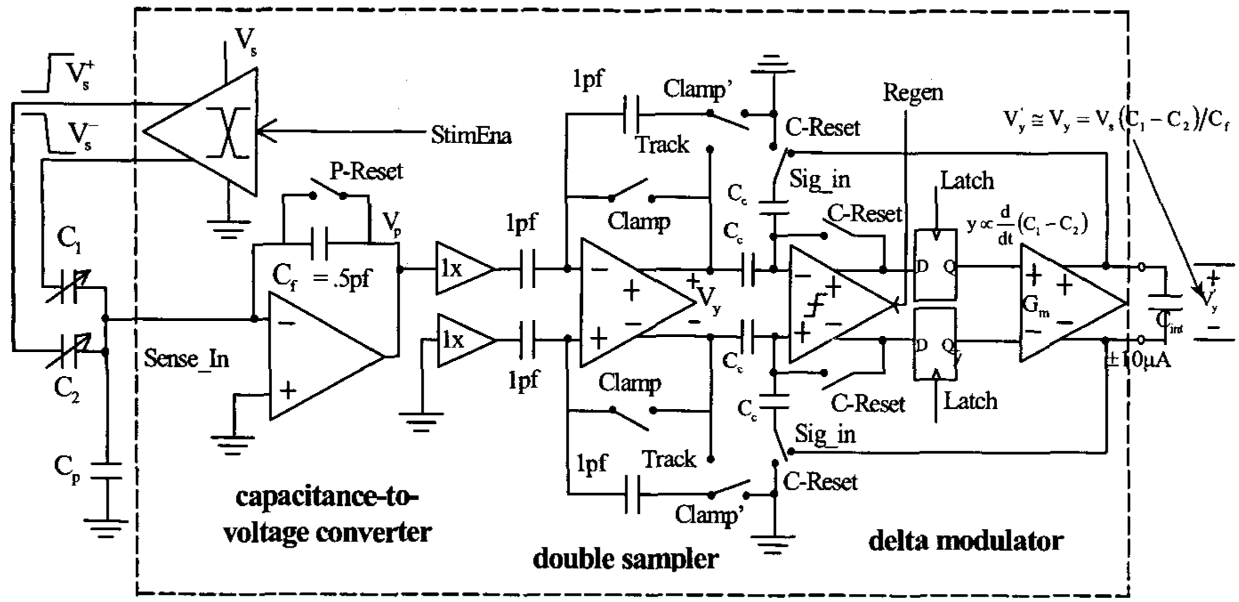

Figure 2: Simplified schematic of the capacitance-to-voltage converter IC.

frequency of 1 MHz. Multi-phase, non-overlapping clock phases (Fig. 3) are produced by an internal clock generator to control the switched-capacitor amplifiers, and cancel opamp offset voltage and charge injection from the CMOS switches. The frontend clocks, Preset, Clamp, and Clamp', have slow falling edges to minimize common-mode charge injection into the summing nodes and avoid charge pumping into the substrate.

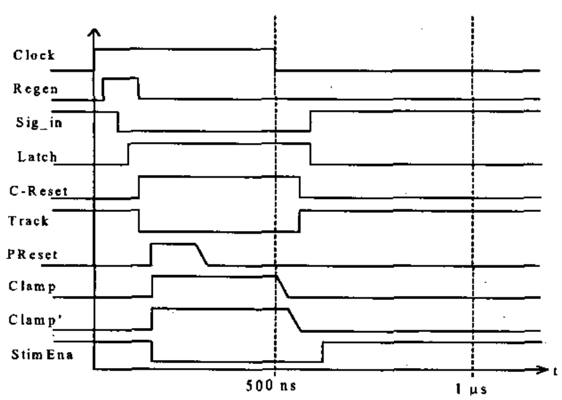

Figure 3: Nominal timing of the internal clock phases.

The final stage of the delta modulator is a continuous-time integrator, implemented using a transconductance opamp. In steady state, the output of this final stage will track changes in sensor capacitance, producing a triangular waveform having a ramp rate of $\pm I_o/C_{int}$, where I_o is the output current produced by the 1b IDAC implemented using an open-loop transconductance opamp, and has a nominal value of 10 μA in this design. C_{int} is an off-chip integration capacitance. Since resolution of the delta modulator is limited by the p-p amplitude of this triangular waveform, the maximum rate of change in sensor capacitance may be traded for resolution, by simply adjusting C_{int}.

The dc transfer characteristic of the converter IC is

$$V_y' = V_s(C_1 - C_2)/C_f\,, \tag{1}$$

where V_y' is the average value of the triangular tracking waveform, V_s is a stimulus voltage and C_f is the feedback capacitor used in the C-to-V amplifier stage. The stimulus voltage V_s is an external input which can be set to any value between 0 and Vdd = 3.5 V. The feedback capacitor is integrated with the amplifier and has a nominal design value of 0.5 pF.

The p-p amplitude of the triangular tracking waveform is

$$V_{p-p} = T_c I_o / C_{int}\,, \tag{2}$$

where T_c is the period of the oversampling clock, nominally 1 μsec in this design. A *pessimistic estimation* of the quantization-limited capacitance resolution is the rms value of the triangular tracking waveform, $V_{p-p}/\sqrt{12}$, divided by the sensitivity, V_s/C_f, i.e.

$$C_q \cong \tfrac{1}{\sqrt{12}}(V_{p-p}/V_s)C_f\,. \tag{3}$$

Thus, with C_{int} = 1 nF, for example, V_{p-p} = 10 mV and quantization-limited resolution is approximately 410 aF. The maximum rate of output voltage change is 10 V/msec, corresponding to a 1-V p-p sinusoid with a maximum frequency of 3.2 kHz. Resolution can be improved at the expense of bandwidth, and vice versa, by adjusting C_{int}.

3. DETAILED DESIGN

3.1 Pre-amplifier

A transconductance opamp, shown in Fig.4, is chosen for the pre-amplifier in the capacitance-to-voltage converter stage. The fully differential topology is used to obtain the best possible PSRR, CMRR, and immunity to interference, with small sacrifices to noise, area, and power. The size and current for the input pair ($M_{1,2}$) are selected based on the consideration of noise, which, referred to the pre-amplifier output, is

$$\overline{V_{on}^2} = 2\times\left(\frac{C_f + C_{in} + C_p + C_{gs}/2 + C_{gd}}{C_f}\right)^2 \times \frac{8}{3}kT\Big/g_{m1,2}\times B\times \pi/2 \quad (2)$$

where C_{in} is the total capacitance associated with the differential sensor, C_{gs} and C_{gd} represent the small-signal capacitance of the input transistors, C_p is the input parasitic capacitance, g_{m1} is the transconductance of the input transistor, and B is the noise bandwidth. The noise bandwidth is set by the 2^{nd}-stage double sampler.

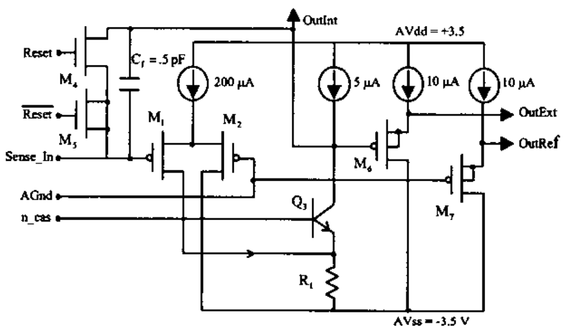

Figure 4: Simplified schematic of the transconductance pre-amplifier.

The theoretically best capacitance resolution, as limited by frontend noise, can be computed by dividing the rms value of the pre-amplifier output noise voltage (equation 2) by the sensitivity, V_s/C_f (from equation 1), and *multiplying by* $\sqrt{2}$ *to account for double sampling.* Using nominal design values V_s = 3.5 V, C_f = 0.5 pF, ($C_{gs}/2$+ C_{gd}) = 1.5 pF, $g_{m1,2}$ = 1 mmho, and B = 6 MHz, and a worst-case package capacitance of (C_{in} + C_p) = 20 pF, the thermal-noise-limited resolution is 130 aF. Therefore, resolution is limited by quantization, given these system parameters.

The preamp functions as a charge integrator with M_4 serving as the reset switch and M_5 is a half-size dummy switch, used to reduce charge injection from the reset switch. The output of the pre-amplifier is buffered by a source follower to minimize capacitive loading, such that the dominant pole of the pre-amplifier is determined by C_{in} and C_p, and the first non-dominant pole is caused by the high capacitance at the drain of M_1. The non-dominant pole has been set to adequately high frequency by the use of a high-g_m BJT cascode transistor.

All required bias voltages and currents for this and all other amplifiers are provided by an on-chip bandgap reference circuit (not shown).

3.2 Double sampling amplifier

A fully differential transconductance opamp (Fig. 5) is used at the core of the double sampling stage. M_1 and M_2 form the differential input pair for the amplifier, M_{11} and M_{12} are folded cascode transistors, and C_{1-4} serve as compensation capacitors. M_{3-6} are the input transistors of the continuous-time common-mode feedback amplifier, and C_1 and C_2 are compensation capacitor for this loop. The bandwidth of differential loop is given by

$$B = g_{m1,2}/(C_1 + 2\cdot C_3) \quad (3)$$

where $g_{m1,2}$ is the transconductance of M_1 and M_2. The bandwidth in this design is nominally 6 MHz, to permit accurate setting at the 1-MHz oversampling clock rate.

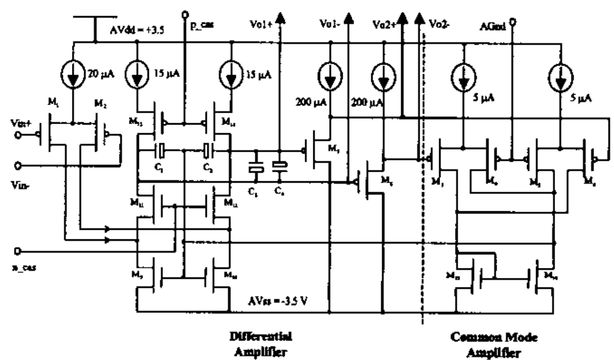

Figure 5: Simplified schematic of the fully differential opamp used in the double-sampling amplifier.

3.3 Comparator

The delta modulator consists of uses a switched-capacitor comparator with built-in offset cancellation. The comparator uses a differential pre-amplifier with latching output stage, as illustrated in Fig. 6. This circuit operates using a 5-V logic supply, and therefore also serves as a level converter between ±3.5-V analog amplifiers and 5-V digital logic.

The comparator operates in two modes, amplification and regeneration. In the amplification mode, the supply current sources (I_1 and I_2) flow through M_1 and M_2, and the differential input voltage signal is amplified by the differential amplifier to increase the signal level by a factor of about 100. In the regeneration mode, the supply current is steered into M_3 and M_4, and a positive feedback regenerates the signal to rail-to-rail voltage. The regeneration time constant is

$$\tau_{reg} = C_{d3}/g_{m3} \approx 1\,ns \quad (4)$$

where C_{d3} is the capacitance at the drain of M_3 and g_{m3} is the transconductance of M_3.

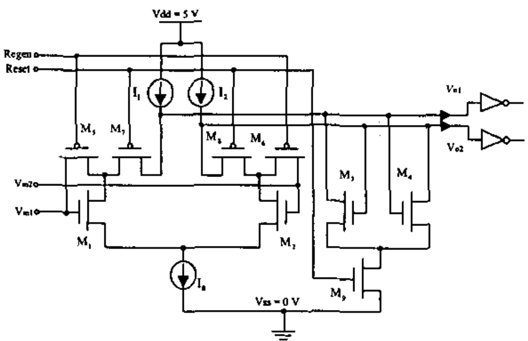

Figure 6: Simplified schematic of the switched-capacitor comparator.

3.4 Integrator

The final stage of the delta modulator is a fully differential continuous-time integrator that employs an open-loop transconductance amplifier and external load capacitor (Fig. 7). The input to the amplifier is a diode-limited binary switching signal that saturates the differential input stage to produce a constant output current ($I_o = \pm 10$ uA) as per the polarity of the input. The differential output current charges the external capacitor at a rate of I_o/C_{int}. Common-mode feedback stabilizes the absolute level of the differential output.

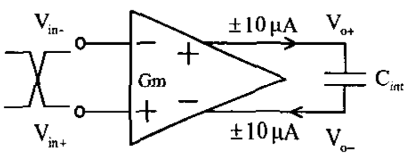

Figure 7: Simplified schematic of the integrator.

4. SiC MEMS RESONATOR

Electrostatically actuated, lateral resonators designed to operate in the kHz frequency range were surface micromachined from single crystal 3C-SiC thin films using novel SiC-on-insulator wafers as the starting substrates. Single crystal 3C-SiC was selected as the main structural material in hopes of creating resonant devices with extremely high mechanical quality factors.

Single crystal 3C-SiC films can readily be grown on Si substrates, but not so on convenient sacrificial layers such as SiO_2. To address this issue, a wafer bonding and etch back technique was used to transfer 3C-SiC films originally grown on Si handle wafers to thermally oxidized Si device wafers, thus creating SiC analogs to conventional SOI wafers [8]. The 3C-SiC films were heteroepitaxially grown on (100) Si handle wafers using a 3 step, carbonization-based atmospheric pressure chemical vapor deposition process detailed elsewhere [9]. Bonding involved a series of mechanical and chemical surface treatments as well as a high temperature annealing step. After bonding, removal of the Si handle wafer was performed in an aggressive Si etchant. These "SiCOI" wafers were then used as substrates for resonator fabrication.

Fabrication of single layer lateral resonators was performed using conventional photolithography and reactive ion etching (RIE). Since the SiC RIE process aggressively attacks photo resist, an Al thin film patterned by lift-off was used as an etch mask. Following SiC RIE, the devices were released by dissolving the SiO_2 layer beneath the shuttle and trusses in HF. After release, the devices were mounted on the test circuit PCB and wire bonded to the appropriate contact pads. A SEM micrograph of a 3C-SiC resonator is shown in Fig. 8.

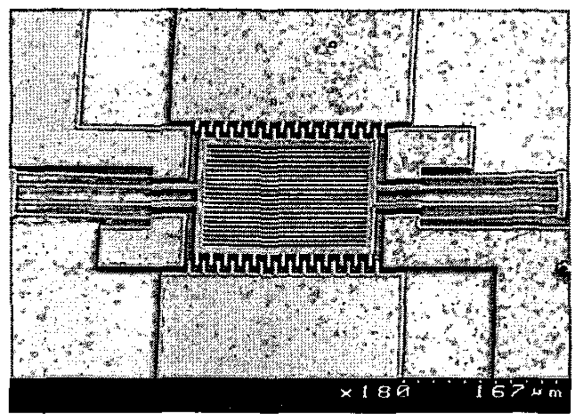

Figure 8: SEM micrograph of a released 3C-SiC lateral resonator.

5. EXPERIMENTAL RESULTS

The C-to-V converter IC has been fabricated through MOSIS using the AMI 1.5-μm CMOS double-polysilicon technology. Some dice were packaged in a 40-pin ceramic DIP for ease of testing, while others were left unpackaged for use in MEMS tests. A photomicrograph of the die is shown in Fig. 9.

The C-to-V converter IC was tested using trim-caps for dc performance and varactors for ac performance. In all tests, the oversampling clock was set to 1 MHz and the reference stimulus was set to 3.5 V for a nominal sensitivity of 7.0 mV/fF. The feedback capacitor was set to 1 nF to permit a maximum signal frequency of 3.2 kHz for output amplitudes of 1 V p-p. Data was acquired using a DVM with a sampling rate of 6 ksps and built-in anti-alias filter.

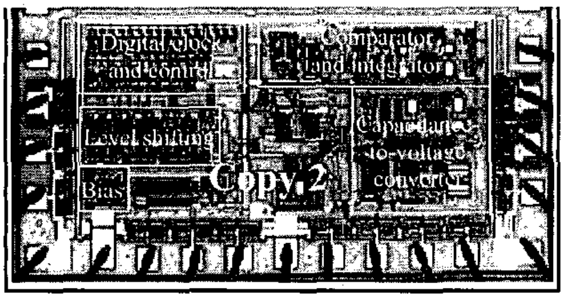

Figure 9: Photomicrograph of the C-to-V converter IC.

The measured dc transfer characteristic, as computed by averaging the 6-ksps DVM samples, is shown in Fig. 10. The measured resolution, as determined by computing the standard deviation of the 6-ksps DVM samples, is shown in Fig. 11. The dynamic range is 68 dB and the nonlinearity error is 0.16%, apparently limited by the trim-caps used for this test. Fig. 11 includes a comparison of resolution and sample rate for this approach with others reported in the literature, clearly indicating the performance and flexibility of this oversampling approach.

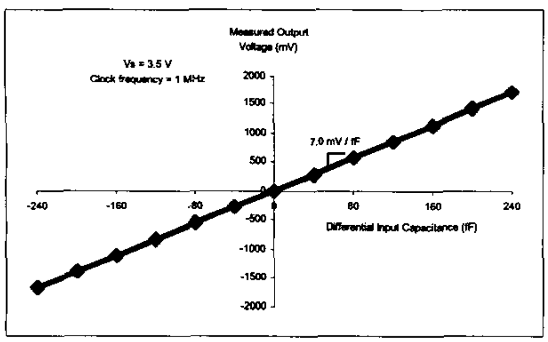

Figure 10: Measure dc transfer characteristic. Offset was calibrated to zero using a trim-cap.

The ac performance of the converter IC was measured using a varactor diode to produce a time-varying capacitance showed excellent linearity in reproducing the sinusoidal capacitance variation and no apparent bandwidth limitation in the frequency range tested, i.e. 3 Hz to 3 kHz.

MEMS resonators were fabricated from 3C-SiC-on-SiO_2 and released using a timed HF etch. In the orientation shown in Fig. 8, the shuttle vibrates top to bottom between two pairs of interdigitated electrodes. The shuttle electrically shorts the pads on the left and right sides, so the resonator acts as a 3-terminal device.

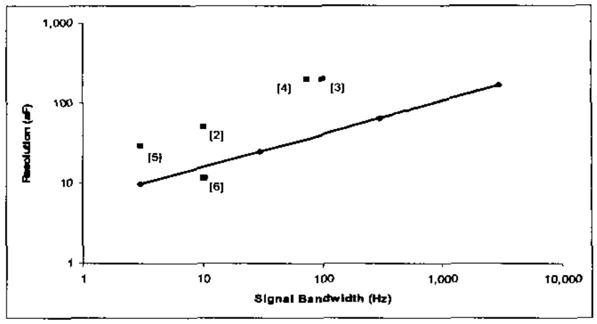

Figure 11: Comparison of measured resolution and bandwidth for various published approaches. The solid line and ▲'s represent measured results from this work, while ■'s are other published results [2-6].

The converter IC and MEMS resonator dice were bonded to a PCB and interfaced using wire bonding and PCB traces. A block diagram of the test set-up is shown in Fig. 12. An ac supply was used to drive the resonator and a dc supply was used to counter the bias force and center the shuttle. The IC was used to measure the capacitance between shuttle and driving pad, which was observed to vary by about ±5 fF, consistent with modeling. The filtered outputs at three different drive frequencies and 760 Torr pressure are shown in Fig.13.

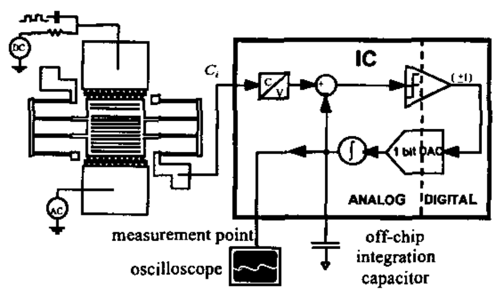

Figure 12: Block diagram of the resonator test setup.

The frequency response of the MEMS device at various pressures was determined by measuring the time-dependent capacitance, shown in Fig. 14. The resonant frequency for this device at all pressures is 16.60 kHz. Q is 51 at 760 Torr, 1000 at 1 Torr, and 6900 at 175 mTorr, illustrating the potential of this resonator for highly stable oscillator circuits. Work continues to achieve lower pressure (and higher Q factors) in the resonator tests.

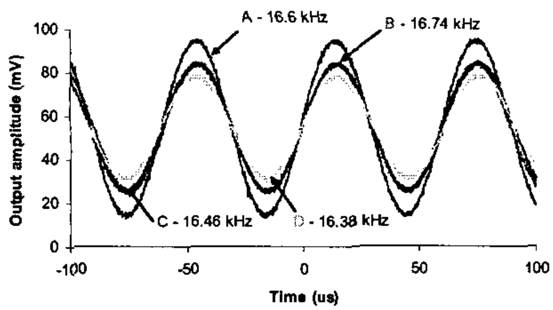

Figure 13: Measured time-domain output for the SiC MEMS lateral resonator test at four drive frequencies near resonance, and 760 Torr pressure. The analog output from the C-to-V converter IC was sampled using a digitizing oscilloscope at 10 Msps, then filtered using a 50-kHz digital low-pass filter.

6. SUMMARY

A capacitance-to-voltage converter IC using correlated double sampling with delta modulator has been developed and used to test the time response of a SiC MEMS resonator. The resolution of the sensing IC can be traded for signal bandwidth to obtain optimum system performance. Work continues to perform tests at reduced pressures and elevated temperatures. The C-to-V converter IC will be an important tool used to evaluate new resonator designs, as well as providing electrical interface to a variety of capacitive sensors for acceleration, pressure, etc.

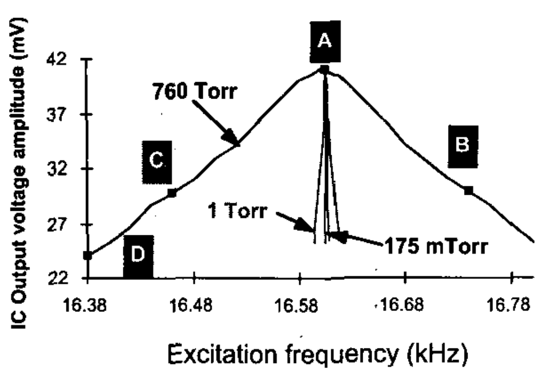

Figure 14: Resonator frequency response at three different pressures. Data points A-D correspond to curves A-D in Fig. 13. Point A represents the maximum amplitude, and B and C are lower by 3 dB.

7. REFERENCES

[1] Bramanti, M., "A high sensitivity measuring technique for capacitive sensor transducers", *IEEE, Trans. On Industrial electronics*, vol. 37, No. 6. pp. 584-586, Dec. 1990.

[2] Toth, F.N., Meijer, G.C.M; and Kerkvliet, H.M.M., "A very accurate measurement system for multielectrode capacitive sensors", *IEEE Trans. on Instrumentation and Measurement*, vol. 45, No. 2, pp 531-535, April, 1996.

[3] Goes, F.M.L.V., and Meijer, G.C.M., "A novel low-cost capacitive-sensor interface", *IEEE, Trans. on Instrumentation and Measurement*, vol. 45, No. 2, pp. 536-540, April, 1996

[4] Mochizuki, K., Masuda, T., and Watanabe, K., "An Interface circuit for high-accuracy signal processing of differential-capacitance transducers", *IEEE Instrumentation and Measurement Technology Conference*, Brussels, Belgium, pp. 1200-1204, June 4-6, 1996.

[5] Kung, J.T., Mills, R.N., and Lee, H.S., "Digital cancellation of noise and offset for capacitive sensors", *IEEE Trans. on Instrumentation and Measurement*, vol. 42, No. 5, pp. 939-942, Oct. 1993.

[6] Marlow, B.K., Greager, D.C., and Moore, M.B., "Highly sensitive capacitance measurement for sensors", *Electronics Letters*, Volume: 2921, 14 Oct. 1993, pp. 1844-1845.

[7] S. Ranganathan, M. Inerfield, S. Roy, and S.L. Garverick, "Sub-Femtofarad Capacitive Sensing for Microfabricated Transducers Using Correlated Double Sampling and Delta Modulation *IEEE Trans. Circuits Sys.—II*, vol. 47 (11), pp. 1170-76, Nov. 2000.

[8] S. Stefanescu, A.A. Yasseen, C.A. Zorman, and M. Mehregany, "Surface micromachined lateral resonant structures fabricated from single-crystal 3C-SiC films", *Proc. 10th Inter. Conf. on Solid State Sen. Act.* –, Sendai, Japan, pp. 194-198, June 7-10, 1999.

[9] C.A. Zorman, A.J. Fleischman, A.S. Dewa, M. Mehregany, C. Jacob, S. Nishino, and P. Pirouz, "Epitaxial growth of 3C-SiC films on 4 in. diameter (100) silicon wafers by atmospheric pressure chemical vapor deposition", *J. Appl. Phys.*, vol. 78, pp. 5136-5138, 1995.